Layering Algorithms For Single-Row Routing

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Abstract—**We develop two fast algorithms for the layering problem that arises when the single-row routing approach to wire layout is used. Both of these algorithms are for the case when the upper and lower street capacities are two. While neither of these algorithms guarantees the production of an optimal layering, it has been empirically determined that both will produce better layerings than an earlier proposed algorithm [13] for this problem. In addition, our algorithms run much faster than the earlier algorithm.**

Keywords and Phrases: **Single-row routing, layering.**

I. Introduction

A SYSTEMATIC approach to the interconnection problem of large multilayer printed circuit boards in which pins and feedthroughs are uniformly spaced on a rectangular grid has been proposed. This approach consists of a systematic decomposition of the general multilayer wiring problem into a number of independent single-layer, single-row routing problems. There are five phases in this decomposition [11], [8]:

1) via assignment,
2) linear placement of via columns,
3) layering,
4) single-row routing,
5) via elimination.

In this paper, we are concerned only with the third and fourth phases: layering and single-row routing. We are given a set $V = \{1, 2, \cdots, n\}$ of n nodes that are evenly spaced along a straight line; and a set $L = \{N_1, N_2, \cdots, N_m\}$ of m nets. Each net N_i represents a set of nodes that are to be made electrically equivalent. The nets satisfy the following conditions:

(i) $N_i \cap N_j = \varnothing \quad i \neq j$

(ii) $\bigcup_{i=1}^{m} N_i = \{1, 2, \cdots, n\}$.

The nodes may be regarded as vias/pins that penetrate all layers of the multilayer board.

Node j, $j \in N_i$ is a *touch point* of net i. The nets are to be realized in a minimum number of layers by the use of nonoverlapping wires that are composed solely of horizontal and vertical segments. Fig. 1(a)–(c) shows some of the legal ways to realize the net $\{1, 3, 6, 9\}$ on a single layer. The wire layout must satisfy the additional requirement that a vertical cut made at any point along the axis formed by the nodes intersect, at most, one horizontal segment from each net. Thus, the wiring of Fig. 1(d) is illegal. Another constraint is that no two conductor paths for two distinct nets have a common electrical junction.

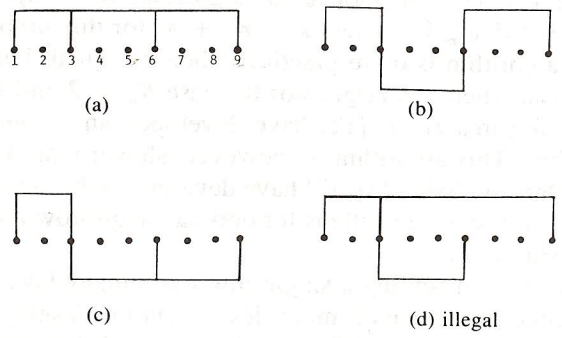

Fig. 1.

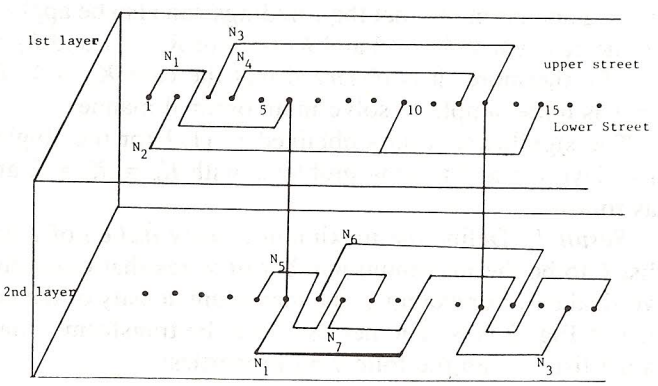

Fig. 2.

The area above the line of nodes is called the *upper street* while that below this line is the *lower street*. Each street has *tracks* that run parallel to the line of nodes (Fig. 2). Horizontal wire segments must be layered in tracks and no track may hold more than one wire segment at any point (of course, several nonoverlapping wire segments may be packed into the same track). Let K_u and K_l denote the number of tracks in the upper and lower streets, respectively. Fig. 2 shows one way to realize a net list $L = \{(1, 6, 11), (2, 10, 15), (3, 13, 16), (4, 12), (5, 9), (7, 14), (8, 17)\}$ on two layers, both of which have $K_u = K_l = 2$.

Much work has been done on the development of fast algorithms to route a single row on a single layer. Kuh *et al.* [5] and Tsukiyama *et al.* [12] have developed neces-

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