Enhanced heuristic for multichannel optimization in gate array layout

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Enhancements to the multichannel optimization heuristic proposed by Aoshima and Kuh[1] for gate array layout are presented. These enhancements result from the introduction of spacing and windowing concepts.

computer-aided design, multichannel optimization, gate arrays

In the multichannel optimization problem[1], a chip in which the cells (or macros) are placed in uniformly separated rows is given (Figure 1). There is a horizontal routing channel between each pair of adjacent cell rows. Vertical routing is performed on the second layer. Each cell row has uniformly spaced terminals on either side. Terminals are labelled $-1, 0, 1, 2, \ldots, k$, where k is the number of nets. If a terminal is labelled i, $1 \leqslant i \leqslant k$, then it is a terminal of net i. A blocked terminal is labelled -1 and a feedthrough location is labelled 0. This model is the same as that used for standard cell and polycell LSI placement and routing[2]. However, in the case discussed here the placement has already been carried out.

The objective of the multichannel optimization problem is to decompose the nets in such a way that they can be routed using horizontal routing channels of least capacity (all channels are assumed to have the same capacity). Each net is decomposed into a set of subnets such that each subnet consists solely of terminals on either side of the same routing channel and the union of the subnets is the original net. Following this decomposition, each routing channel is routed independently of the others using a classical channel router. When a channel is being routed, all subnets with end points on that channel are considered.

Since the output of the multichannel optimization problem is the input for classical channel routing, and since channel routers are generally able to route using as many tracks as the channel density[3,4], it is reasonable to modify the objective of the multichannel optimization problem to the following: 'decompose the nets so that the maximum density in any channel is a minimum'.

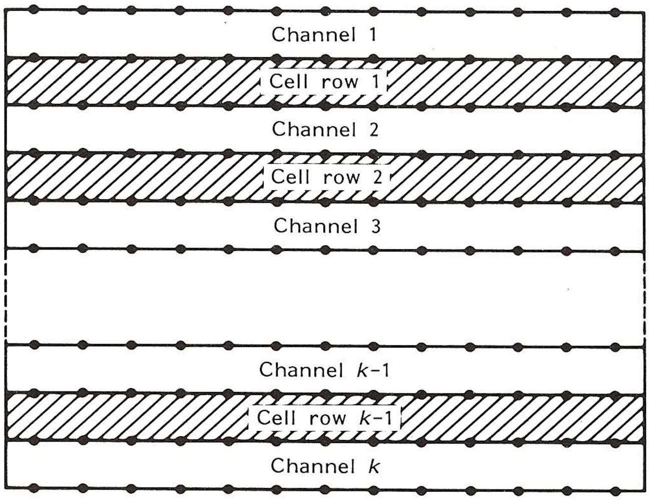

Figure 1. Chip with cells placed in uniformly separated rows

For this objective function, Aoshima and Kuh[1] have proposed two heuristics, namely, optimum decomposition and practical approach. In both of these, net decomposition is performed one net at a time. When a net is being decomposed, available information about the decomposition of all other nets is used. One complete iteration of each heuristic involves decomposing or modifying the decomposition of each of the nets. As many iterations of each heuristic as desired can be performed. The heuristic may be terminated either when an iteration does not improve the decomposition (i.e. does not reduce the maximum channel density) or when the available computation resources are exhausted.

HEURISTICS OF AOSHIMA AND KUH

Optimum decomposition

In the optimum decomposition heuristic of Aoshima and Kuh[1], a graph $G_n = (V_n, E_n)$ is constructed for the net n that is to be decomposed. The vertices V_n of G_n include all terminals of net n together with the available feedthroughs. (i, j) is an edge of E_n only if the terminals

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