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A new VLSI system for adaptive recursive filtering *

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Abstract. We develop an efficient bidirectional chain VLSI system for the adaptive recursive filtering problem. Our design is an improvement over previous designs. It matches the performance of a broadcast chain but does not use the broadcast capability.

Keywords. VLSI architectures, systolic systems, adaptive recursive filtering.

1. Introduction

VLSI architectures for a variety of problems have been proposed by several authors. A bibliography of over 150 research papers dealing with this subject appears in [6]. In this paper, we are concerned solely with the adaptive recursive filtering problem. The input to this problem is an $n \times w$ matrix A of weighting coefficients and a $1 \times w$ vector $(x_{1-w}, \ldots, x_0)$. The output is a $1 \times n$ vector $(x_1, \ldots, x_n)$ where

$$x_i = \sum_{j=1}^{w} a_{ij} x_{i+j-w-1}, \quad i = 1, 2, \ldots, n. \tag{1}$$

In evaluating a VLSI design, we assume that the VLSI system will be attached to the host processor using a bus as in Fig. 1. The evaluation of a VLSI design should take the following into account:

(1) *Processors*: how many processors are used in the VLSI system? This figure is denoted by P.

(2) *Bus bandwidth*: the maximum amount of data to be transmitted between the host and the VLSI system in any cycle. This figure is denoted by B.

(3) *Speed*: how much time does the VLSI system need to complete its task? This time may be decomposed into the times T_C (time for computations) and T_D (time for data transmissions both within the VLSI system and between the host and the VLSI system).

Let C denote the time spent for computation by a single processor algorithm and D denote the total amount of data that needs to be transmitted between the host and VLSI system. As an example, consider the problem of multiplying two $n \times n$ matrices A and B to get Y. Each element of Y is the sum of n products. We shall count one multiplication and addition as one arithmetic (or computation) step. If the classical matrix multiplication algorithm is used, $C = n^3$. If $P = n$, then $T_C \geqslant n^2$. The host needs to send $2n^2$ elements to the VLSI system and

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