Parallel Processing for Artificial Intelligence 1
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Chapter 4

Image Processing On Reconfigurable Meshes With Buses*

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Abstract

In this chapter, we describe different reconfigurable mesh with buses architectures and show how several image processing problems can be solved efficiently on the weakest of these. The specific problems considered are: area and perimeter of components, shrinking and expanding, clustering, and template matching. In many cases, the resulting algorithms are faster than those for other parallel computer architectures.

1. Introduction

Recently, several researchers have proposed a modification to the well studied mesh architecture in which the interprocessor links are replaced by a reconfigurable bus. The resulting parallel computer architecture is called a reconfigurable mesh with bus (RMB). In all two dimensional $N \times N$ RMB computers, the N^2 processors are located at the N^2 grid points of an $N \times N$ grid (just as in a traditional mesh computer). However, the traditional linkage between mesh adjacent processors is absent. Instead, interprocessor communication takes place via a reconfigurable bus. The RMB family of architectures includes the RMESH, PARBUS, polymorphic torus, and the mesh reconfigurable network (MRN). The architectures have become popular because they are ralatively easy to program and because many problems can be solved very efficiently on them. In fact, it is possible to solve some problems faster on an RMB computer than is theoretically possible on a PRAM computer (See for example: [10, 34, 35, 39]).

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