Guest Editors' Introduction: Special Section on System-Level Design and Validation of Heterogeneous Chip Multiprocessors

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EMERGING multicore architectures, especially Chip Multi-Processors (CMPs) and Multiprocessor Systems-on-Chip (MPSoC), are used in a wide variety of systems. They are necessary to avoid the unsustainable power consumption profile of increasing clock speed of uniprocessors in the early part of the last decade. The designers are thus forced to employ innovative design alternatives such as heterogeneous cores, novel network-on-chips, GPUs, and reconfigurable fabrics. At the same time, the design teams face shortened design cycles and the increasing pool of immediate users, as a large variety of such systems are already placed in the hands of consumers (including Motorola Xoom, Apple iPad, to name a few). To meet such stringent constraints and to guarantee quality of the products, the emerging CMPs need to be designed by making verification of the functionality as an integral part of the design methodology from inception to final product delivery, which presents a design paradigm shift. Until now the architectural exploration and initial performance evaluation phases were prior to the design, whereas the validation tasks were employed after the design is completed. Now, more than ever, validation must be done at every stage of the design, and as the designs move from one level of abstraction to the next, consistency must be validated as well.

Various studies indicate that the functional verification of complex CMPs consumes majority (as much as 70 percent) of the overall design time and resources and yet many CMP designs exhibit first silicon failure, primarily due to the functional errors. Functional verification complexity is expected to increase further due to the shift to heterogeneous multicore architectures that increasingly use novel interconnect and cache architectures. There are various important challenges to enable closer integration of verification within the overall design cycle including high-level modeling, efficient and scalable verification techniques at different abstraction levels, as well as the aids for application development, including debug support. Eliminating conditions for bugs in the design throughout the process requires consistent and continuous use of system-level modeling and validation.

This issue of *IEEE Transactions on Computers* includes a special section dealing with the system-level design and validation of heterogeneous chip multiprocessors. The creation of the section was motivated by a lively discussion at the IEEE High-Level Design Validation and Test (HLDVT - http://www.hldvt.com) at Napa Valley in 2011. Three papers were selected in this special section through rigorous review process from a set of high quality submissions consisting of regular papers as well as selected HLDVT'11 papers.

The first article, "Automatic Generation of Transducer Models for Bus-Based MPSoC Design," by Hansu Cho, Lochi Yu, and Samar Abdi, presents a flexible, scalable and efficient communication module (transducer) that supports inter-PE communication in a bus-based MPSoC system. The authors define the transducer architecture and methods for automatically generating a synthesizable model of the transducer from a system-level specification. The authors demonstrate that automatic transducer generation avoidsthe time consuming and error prone task of manual communication modeling in MPSoC systems.

The second article, "UNIVERCM: the UNIversal VERsatile Computational Model for Heterogeneous System Integration," by Luigi Di Guglielmo, Franco Fummi, Graziano Pravadelli, Francesco Stefanni and, and Sara Vinco, presents a framework for efficiently supporting bottom-up design and system integration from a set of heterogeneous components. The framework exploits an interchange format and a set of related tools for automatically mapping heterogeneous descriptions to a homogeneous representation. The authors demonstrate that the SystemC code generated from the UNIVERCM model preserves the accuracy achievedby traditional top-down approaches and leads to significant speedup compared to the heterogeneous simulation.

The third article, "Post-Silicon Code Coverage for Multiprocessor System-on-Chip Designs," by Kyle Balston, Mehdi Karimibiuki, Alan J. Hu, André Ivanov, and Steven J.E. Wilton, presents a novel and scalable method for coverage monitoring. The authors are able to obtain a number of metrics dealing with the coverage and the associated costs, both in pre and post-silicon stages. The authors demonstrate a clear and interesting distinction between pre and post-silicon coverage. As a special testament to the scalability, the authors are able to evaluate coverage while booting an OS on silicon.

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Finally, we would like to take the opportunity to thank the contributing authors, reviewers, the editorial staff at IEEE, and the Editor-in-Chief, Professor Albert Y. Zomaya. Without their support, this special section would not be possible.

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Guest Editors

Zeljko Zilic is an associate professor at McGill University, Montreal, QC, Canada. Professor Zilic has worked at Lucent Technologies in 1997-1998 and used a sabbatical leave in 2004/2005 to work with ST Microelectronics in Ottawa on assertion-based verification of multiprocessors on chip, conducted in cooperation with the IBM research lab in Haifa. Professor Zilic conducts research on various aspects of the quality-driven design of embedded heterogeneous microsystems. He has coauthored three books, five patents and over 200 papers, for which he received several awards, including Myril B. Reed Best Paper award from Midwest Symposium on Circuits and Systems, and Best Paper Award from Design and Verification Conference and Exposition (DVCon). He was voted by National Council of Deans of Engineering to receive Wighton Fellowship for his embedded system design teaching in 2006. He has been the guest editor for a special issue of *IEEE Design and Test Magazine* on Transaction-level Validation of Multicore Architectures in 2011 and for *VLSI Design* special issue on Advances in Formal Hardware and System Validation in 2013. He is a senior member of IEEE and ACM.

Prabhat Mishra is an associate professor at University of Florida, Ganesville, USA. His research interests include design automation of embedded systems, energy-aware computing, and hardware verification. He received his PhD from the University of California, Irvine in 2004. He has published four books, ten book chapters and more than 100 research articles in premier international journals and conferences. His research has been recognized by several awards including the NSF CAREER Award from the US National Science Foundation, two best paper awards (VLSI Design 2011 and CODES+ISSS 2003), and 2004 EDAA Outstanding Dissertation Award from the European Design Automation Association. Professor Mishra currently serves as an associate editor of *ACM Transactions on Design Automation of Electronic Systems*, *IEEE Design & Test of Computers*, *IET Computers & Digital Techniques*, and *Journal of Electronic Testing*, and as a technical program committee member of several ACM and IEEE conferences including DAC, ICCAD, DATE, ASPDAC, CODES+ISSS, RTAS and VLSI Design. He is a senior member of both ACM and IEEE.

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