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Guest Editorial

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Increasing design complexity coupled with the use of nanometer-scale electronics create a critical need for the development of innovative techniques for high-level design validation and test. High-level approaches are promising to significantly improve the design quality as well as to drastically reduce the overall validation and test effort. Simulation-based validation cannot guarantee correctness due to extremely large, potentially infinite, number of input combinations. On the other hand, formal methods can guarantee correctness for small designs but are unsuitable for multi-million gate designs due to state space explosion. There is a need for novel tools, techniques and methodologies that can verify extremely large designs using a combination of simulation based techniques and formal methods. Similarly, use of highly unreliable nano-electronics creates an opportunity to develop novel approaches for post-silicon validation, test and debug to ensure that the manufactured device is reliable and has the expected behavior. Efficient approaches for addressing these challenges are presented in this special issue, containing nine selected papers, whose preliminary versions were presented at the *IEEE High Level Design Validation and Test Workshop*.

The nine papers of this special issue are classified into three categories, which are high-level testing and debug approaches, simulation-based validation methods, and formal verification techniques.

The first four papers relate to high-level models and methods for silicon testing and diagnosis. The first paper by Fang et al. exploits the advantages of using functional test sequences to target defects that are not detected by structural test and presents a design-for-testability method that uses the register-transfer level output deviations metric to select observation points to improve defect coverage. The second paper by Chandrasekar et al. proposes efficient techniques for diagnostics test pattern generation using incremental learning and output deviation based X-filling of the test patterns with the objective of enhancing the test set's diagnostic ability. The third paper by Fan et al. investigates the topic of accelerating the jitter and bit-error-rate testing in high speed serial interfaces and presents a jitter tolerance extrapolation algorithm as well as a low cost external loopback-based testing scheme. The fourth paper by Gulati et al. presents an efficient approach for implementation of fault table generation on a graphics processing unit by utilizing both bit-parallelism and thread-level parallelism.

The next two papers address the challenges associated with high-level modeling, analysis and validation of complex systems. Tong et al. rely on the duality between property checkers and test generators to take advantage of the information present in the assertions to generate efficient test sequences for simulation-based validation. Xue et al. analyze the scheduling problem using periodic clock calculus to compute the throughput of latency insensitive systems, and also propose a method to synthesize fractional synchronizers to equalize cycles with different throughputs.

The last three papers are related to efficient design verification using formal methods. Moon et al. present efficient algorithms to learn invariants from approximate constraint solving and apply these learned invariants for formal property checking. Cabodi et al. exploit incremental satisfiability, by iteratively refining the set of candidate transformations with a counter-example driven analysis, until an unsatisfiable point is reached in order to search for multiple equivalence-preserving transformations of combi-

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national circuits. The last paper by Verdoolaege et al. investigates the applicability of existing loop and data transformation techniques for performance improvement in multimedia systems, and presents an extension of a widening based approach to handle accesses to array slices, data dependent accesses and data dependent assignments.

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Prabhat Mishra received B.E. degree from Jadavpur University, India in 1994, the M.Tech. degree from the Indian Institute of Technology, Kharagpur in 1996, and the Ph.D. degree from the University of California, Irvine in 2004—all in computer science. He spent several years with various semiconductor and design automation companies including Texas Instruments, Synopsys, Intel, and Freescale (Motorola). He is currently an Assistant Professor with the Department of Computer and Information Science and Engineering at University of Florida. His research interests include design automation of embedded systems, reconfigurable architectures, and high-level validation. His research has been recognized by various awards, including an NSF CAREER Award in 2008, the EDAA Outstanding Dissertation Award in 2005 and the CODES+ISSS Best Paper Award in 2003. He has published two books, several book chapters, and more than 50 papers in design automation field. Dr. Mishra currently serves as General Chair of IEEE High Level Design Validation and Test workshop, Information Director of ACM Transactions on Design Automation of Electronic Systems, Guest Editor of IEEE Design & Test of Computers, and as a program/organizing committee member of several ACM and IEEE conferences. He is a senior member of the IEEE, and a professional member of ACM.