

The Complexity of Single Row Routing

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Abstract—This paper investigates a systematic suboptimal approach to multilayer rectilinear wire routing: the single row approach. The method involves decomposing the general rectilinear wiring problem into a number of conceptually simpler single row problems. The complexity of the decomposition process is first considered. Under interesting optimization criteria, each step in the decomposition process is shown to be NP-hard. Then the single row wiring problem itself is considered under a variety of optimization criteria. In some cases, either efficient or “usually good” algorithms are possible. In other cases, the problem turns out to be NP-hard.

I. INTRODUCTION

THE fundamental *wire routing problem* occurs at all levels of the physical packaging hierarchy (e.g., within the IC chip, in the multichip package, on the PC card, in the backpanel and sidepanel, etc.). In this basic form, the problem may be stated as follows. We are given a set $W = \{(u_i, v_i)(x_i, y_i) | 1 \leq i \leq n\}$ of n wires. (u_i, v_i) and (x_i, y_i) are the respective coordinates of the end points of wire i , $1 \leq i \leq n$. When more than one layer is available, the wire end-points are assumed to exist on all the layers.¹ The problem is to define the precise conductor paths for each of these wires, using as few layers as possible and subject to the following constraints:

- (1) Each conductor path must be made up of horizontal and vertical segments only (the rectilinear constraint).
- (2) The various conductor paths are not allowed to cross on any given layer.

This problem is NP-hard (for a proof, see [11]). So, it is not surprising that most approaches to the problem have been heuristic in nature (see, e.g., [5], [9], [6], [4] etc.). These approaches have the common characteristic that there is no guarantee of their finding optimal solutions efficiently. Furthermore, being very ad hoc in their various approaches, they give no feel for the inherent difficulty (i.e., the routability²) of the given instance. This makes it very hard to evaluate the suitability of any such heuristic approach for a given mix of routing problems.

This paper presents the results of a thorough investigation of a promising approach to the general wiring problem. This approach is called the *single row approach* [14]. It

¹This assumption reflects certain limitations in early package fabrication technologies. It is a little simplistic in the modern context. However, we shall retain this assumption because: (i) it really impacts only the pre-routing phase of the single row approach; (ii) it represents a simplifying assumption; and (iii) we wish to add to a pool of complexity results that have been obtained using this assumption.

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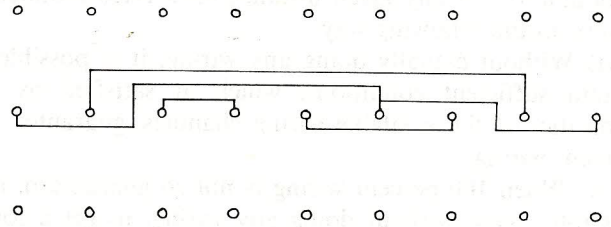


Fig. 1.

is a very systematic (but suboptimal) approach to wiring; it even allows a-priori estimation of the fraction of wires inherently routable. It works best for very large instances of the wiring problem (i.e., containing more than 1000 wires), which usually have reasonably “regular” geometries; i.e., there is a reasonable nontrivial rectangular grid, such that each wire end-point coincides with some grid point. (Of course, it is not necessary that every grid point be so occupied.) We will refer to this imaginary grid as the *point grid*.

Often, there are restrictions as to where vias may exist. In that case, the point grid must be refined so that each legal via location also coincides with some grid point. In any case, the extent of the point grid is limited by the (fixed) area of the wiring surface.

The essence of the single row approach lies in three *strategic constraints* introduced by it:

A) Wires can only connect points (either pins or vias) that are either in the same row or in the same column. This amounts to decomposing the general wiring problem into a number of “single row” wiring problems, one for every row and every column of the point grid.

B) The layout of a wire connecting points in the same row (column) must be confined to the two wiring channels on either side of that row (column). Fig. 1 shows such a layout. So, if the wiring channels have sufficient capacities, the layout of each row (column) is independent of the layout of any other row (column).

C) On any given layer, only rows (columns) can be laid out. So, the layout of any row is independent of the layout of any column, since they will be on different layers. In conjunction with constraint B), this makes each “single row” wiring problem truly independent of any other. Another implication of this constraint is that at least two layers must be available for wiring. (Even when one-layer realizations are possible, the single row approach will use two or

