

CURRICULUM VITAE

Prabhat Mishra

Assistant Professor

*Dept. of Computer and Information Science and Engineering
University of Florida, Gainesville, FL 32611-6120, USA*

Tel: (352) 392 2680

Fax: (352) 392 1220

Email: prabhat@cise.ufl.edu

URL: <http://www.cise.ufl.edu/~prabhat>

RESEARCH INTERESTS: Design automation for embedded and reconfigurable systems, VLSI CAD, hardware/software verification using a combination of simulation-based techniques and formal methods.

EDUCATION

1999-2004: **Ph.D.** in Information and Computer Science, University of California, Irvine, USA.

1994-1996: **M.Tech.** in Computer Science, Indian Institute of Technology, Kharagpur, India.

1990-1994: **B.E.** in Computer Science and Engineering, Jadavpur University, Kolkata, India.

EMPLOYMENT

Jul 16, 2004 – :	<i>Assistant Professor</i>	Computer & Info. Science & Engg., University of Florida
May-Dec 2006:	<i>Assistant Professor</i>	Indian Institute of Science , Bangalore, India
Apr-Jul 2004:	<i>Assistant Project Scientist</i>	Center for Embedded Computer Systems , UC Irvine
1999-2004:	<i>Research/Teaching Assistant</i>	University of California, Irvine , USA
Summer'01+02:	<i>Research Intern</i>	Somerset PowerPC Design Center, Motorola , Austin
Summer 2000:	<i>Research Intern</i>	IA-64 Performance Group, Intel , Santa Clara, California
1998 – 1999:	<i>Senior R&D Engineer</i>	Synopsys , Bangalore, India.
1997 – 1998:	<i>Senior Software Engineer</i>	Sasken , Bangalore, India.
1996 – 1997:	<i>Software Design Engineer</i>	Texas Instruments , Bangalore, India.

AWARDS

1. **NSF CAREER Award**, National Science Foundation, 2008 – 2013.
2. **Best Paper Award Nomination**, ACM/IEEE Design Automation Conference (DAC), 2009.
3. **Best Paper Award Nomination**, International Conference on VLSI Design, 2009.
4. **International Educator of the Year Award**, College of Engineering, University of Florida, 2007.
5. **EDAA Outstanding Dissertation Award**, European Design and Automation Association, 2004.
6. **Best Paper Award**, ACM/IEEE CODES+ISSS Conference, October 2003.
7. **Motorola Silver Quill Award**, 2002.
8. **Regents Fellowship**, University of California, 1999-2000.
9. **18th Rank in West Bengal Higher Secondary Examination** (among 250000 students), India, 1990.
10. **National Scholarships** for merit in 10th and 12th examinations, 1988-1994, Government of India.

SUMMARY OF PUBLICATIONS

- 2 Books, 8 book chapters, and 2 patents (one issued, another pending)
- 16 journal articles, 31 referred conference papers, 10 referred workshop papers with archival proceedings

SELECTED PUBLICATIONS

Books

- B2** P. Mishra and N. Dutt, “*Functional Verification of Programmable Embedded Architectures: A Top-Down Approach*”, **Springer**, ISBN 0-387-26143-5, July 2005.
- B1** P. Mishra and N. Dutt, Editors, “*Processor Description Languages: Applications and Methodologies*”, ISBN 978-0-12-3742872, **Morgan Kaufmann**, June 2008.

Journal Articles

- J16** M. Chen and P. Mishra, Efficient Techniques for Directed Test Generation using Incremental Satisfiability, accepted to appear in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2009.
- J15** X. Qin, C. Murthy and P. Mishra, Decoding-aware Compression of FPGA Bitstreams, Accepted to appear in IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI), 2009.
- J14** K. Basu and P. Mishra, “*Test-Data Compression using Application-Aware Bitmask and Dictionary Selection Methods*”, accepted to appear in IEEE Transactions on Very Large Scale Integration Systems.
- J13** X. Qin and P. Mishra, Efficient Placement of Compressed Code for Parallel Decompression, accepted to appear in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD).
- J12** H. Koo and P. Mishra, Functional Test Generation using Design and Property Decomposition Techniques, ACM Transactions on Embedded Computing Systems (TECS), 8(4), Article 32, July 2009.
- J11** S. Seong and P. Mishra, *Bitmask-Based Code Compression for Embedded Systems*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 27(4), pages 673-685, 2008.
- J10** P. Mishra and N. Dutt, *Specification-driven Directed Test Generation for Validation of Pipelined Processors*, ACM Transactions on Design Automation of Electronic Systems (TODAES), volume 13, no 3, 36 pages, Article 42, July 2008.
- J9** M. Reshadi, P. Mishra and N. Dutt, “*Hybrid Compiled Simulation: An Efficient Technique for Instruction-Set Architecture Simulation*”, ACM Transactions on Embedded Computing Systems (TECS), volume 8, no 3, April 2009.
- J8** P. Mishra, A. Shrivastava and N. Dutt, “*Architecture Description Language (ADL)-driven Software Toolkit Generation for Architectural Exploration of Programmable SOCs*”, ACM Transactions on Design Automation of Electronic Systems (TODAES), volume 11, no 3, pages 1-33, July 2006.
- J7** M. Reshadi, P. Mishra and N. Dutt, “*A Retargetable Framework for Instruction-Set Architecture Simulation*”, ACM Transactions on Embedded Computing Systems (TECS), 5(2), pages 431-452, 2006.
- J6** P. Mishra and N. Dutt, “*Architecture Description Languages for Programmable Embedded Systems*”, IEE Proceedings on Computers and Digital Techniques (CDT), 152(3), pages 285-297, May 2005.
- J5** P. Mishra, N. Dutt, N. Krishnamurthy and M. Abadir, “*A Methodology for Validation of Microprocessors using Symbolic Simulation*”, Inderscience International Journal of Embedded Systems (IJES), 1(1/2), pages 14-22, 2005.

- J4** P. Mishra, N. Dutt, N. Krishnamurthy, and M. Abadir, “A *Top-Down Methodology for Validation of Microprocessors*”, IEEE Design & Test of Computers, 21(2), pages 122-131, March-April, 2004.
- J3** P. Mishra, N. Dutt, and H. Tomiyama, “*Towards Automatic Validation of Dynamic Behavior in Pipelined Processor Specifications*”, Kluwer Design Automation for Embedded Systems (DAES), 8(2), pages 249-265, 2003.
- J2** P. Mishra and N. Dutt, “*Modeling and Validation of Pipeline Specifications*”, ACM Transactions on Embedded Computing Systems (TECS), 3(1), pages 140-162, 2004.
- J1** P. Mishra, M. Mamidipaka, and N. Dutt, “*Processor-Memory Co-Exploration using an Architecture Description Language*”, ACM Transactions on Embedded Computing Systems (TECS), 3(1), pages 114-139, 2004.

Book Chapters

- BC8** N. Bandyopadhyay, K. Basu and P. Mishra, “*HMDES, ISDL and other Contemporary ADLs*”, in *Processor Description Languages: Applications and Methodologies*, Prabhat Mishra and Nikil Dutt, Editors, Morgan Kaufmann Publishers, 2008.
- BC7** P. Mishra and A. Shrivastava, “*ADL-driven Methodologies for Design Automation of Embedded Processors*”, in *Processor Description Languages: Applications and Methodologies*, Prabhat Mishra and Nikil Dutt, Editors, Morgan Kaufmann Publishers, 2008.
- BC6** P. Mishra and N. Dutt, “*EXPRESSION: An ADL for Software Toolkit Generation, Exploration, and Validation of Programmable SOC Architectures*”, in *Processor Description Languages: Applications and Methodologies*, Prabhat Mishra and Nikil Dutt, Editors, Morgan Kaufmann Publishers, 2008.
- BC5** P. Mishra and N. Dutt, “*Introduction to Architecture Description Languages*”, in *Processor Description Languages: Applications and Methodologies*, Prabhat Mishra and Nikil Dutt, Editors, Morgan Kaufmann Publishers, 2008.
- BC4** P. Mishra and N. Dutt, “*Architecture Description Languages*”, in *Customizable and Configurable Embedded Processors*”, Paolo Ienne and Rainer Leupers, Editors, *Morgan Kaufmann*, 2006.
- BC3** P. Mishra and N. Dutt, “*Processor Modeling and Design Tools*”, in *The EDA Handbook*, G. Martin, L. Lavagno, and L. Scheffer, Editors, *CRC Press*, 2005.
- BC2** P. Mishra and N. Dutt, “*Architecture Description Languages for Programmable Embedded Systems*”, in *SOC: Next Generation Electronics*, Bashir M. Al-Hashimi, Editor, *IEE Press*, 2005.
- BC1** P. Mishra and N. Dutt, “*Modeling and Verification of Pipelined Embedded Processors in the Presence of Hazards and Exceptions*”, in *Design and Analysis of Distributed Embedded Systems*, Kluwer Academic Publishers, pages 81-90, 2002.

Referred Conference Papers

- C31** M. Chen, X. Qin and P. Mishra, Efficient Decision Ordering Techniques for SAT-based Test Generation, Design Automation and Test in Europe (DATE), pages -, Dresden, Germany, March 8 - 12, 2010.
- C30** X. Qin, M. Chen and P. Mishra, Synchronized Generation of Directed Tests using Satisfiability Solving, International Conference on VLSI Design, pages -, Bangalore, India, January 3-7, 2010.
- C29** W. Wang and P. Mishra, Leakage-Aware Energy Minimization using Dynamic Voltage Scaling and Cache Reconfiguration in Real-Time Systems, International Conference on VLSI Design, pages -, Bangalore, India, January 3-7, 2010.
- C28** N. Dang, A. Roychoudhury, T. Mitra and P. Mishra, “*Generating Test Programs to Cover Pipeline Interactions*”, ACM/IEEE Design Automation Conference (DAC), pages -, San Francisco, California, USA, July 26-31, 2009. **[Best Paper Award Nomination]**
- C27** W. Wang and P. Mishra, “*Dynamic Reconfiguration of Two-Level Caches in Soft Real-Time Embedded Systems*”, IEEE International Symposium on VLSI (ISVLSI), pages 145–150, May 13-15, 2009.
- C26** C. Murthy and P. Mishra, “*Lossless Compression using Efficient Encoding of Bitmasks*”, IEEE International Symposium on VLSI (ISVLSI), pages 163–168, May 13-15, 2009.
- C25** C. Murthy and P. Mishra, “*Bitmask-based Control Word Compression for NISC Architecture*”, ACM Great Lakes Symposium on VLSI (GLSVLSI), pages 321–326, Boston, May 10–12, 2009.
- C24** X. Qin and P. Mishra, “*Efficient Placement of Compressed Code for Parallel Decompression*”, International Conference on VLSI Design, pages 335–340, New Delhi, India, January 5-9, 2009.
- C23** W. Wang, P. Mishra and Ann Gordon-Ross, “*SACR: Scheduling-Aware Cache Reconfiguration for Real-Time Embedded Systems*”, International Conference on VLSI Design, pages 547–552, New Delhi, India, January 5-9, 2009.
- C22** P. Mishra and M. Chen, “*Efficient Techniques for Directed Test Generation using Incremental Satisfiability*”, International Conference on VLSI Design, pages 65–70, New Delhi, India, January 5-9, 2009. **[Best Paper Award Nomination]**
- C21** H-M. Koo and P. Mishra, “*Specification-based Compaction of Directed Tests for Functional Validation of Pipelined Processors*”, ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), pages 137–142, Atlanta, USA, October 19 - 24, 2008.
- C20** K. Basu and P. Mishra, “*A Novel Test-Data Compression Technique using Application-Aware Bitmask and Dictionary Selection Methods*”, ACM Great Lakes Symposium on VLSI (GLSVLSI), pages 83–88, Orlando, May 4 – 6, 2008.
- C19** M. Chen and P. Mishra, “*Coverage-driven Automatic Test Generation for UML Activity Diagrams*”, ACM Great Lakes Symposium on VLSI (GLSVLSI), pages 139–142, Orlando, May 4 – 6, 2008.
- C18** S. Seong and P. Mishra, “*An Efficient Code Compression Technique using Application-Aware Bitmask and Dictionary Selection Methods*”, Design Automation and Test in Europe (DATE), 582 – 587, 2007.

- C17** H-M. Koo and P. Mishra, “Automated Micro-architectural Test Generation for Validation of Modern Processors”, US-Korea Conference on Global Challenges in Science and Technology (UKC), Washington DC, August 9-12, 2007.
- C16** X. Li, A. Roychoudhury, T. Mitra, P. Mishra and X. Cheng, “A Retargetable Software Timing Analyzer Using Architecture Description Language”, Asia and South Pacific Design Automation Conference (ASPDAC), pages 396-401, 2007.
- C15** S. Seong and P. Mishra, “A Bitmask-based Code Compression Technique for Embedded Systems”, IEEE/ACM International Conference on Computer Aided Design (ICCAD), pages 251 – 254, 2006.
- C14** H. Koo and P. Mishra, “Test Generation using SAT-based Bounded Model Checking for Validation of Pipelined Processors”, ACM Great Lakes Symposium on VLSI (GLSVLSI), pages 362-365, 2006.
- C13** H. Koo and P. Mishra, “Coverage-driven Functional Test Generation for Processor Validation using Formal Methods”, US-Korea Conference on Science, Technology, and Entrepreneurship (UKC), 2006.
- C12** H. Koo and P. Mishra, “Functional Test Generation using Property Decompositions for Validation of Pipelined Processors”, Design Automation and Test in Europe (DATE), pages 1240-1245, 2006.
- C11** M. Reshadi and P. Mishra, “Memory Access Optimizations in Instruction-Set Simulators”, International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), pages 237-242, 2005.
- C10** P. Mishra and N. Dutt, “Functional Coverage Driven Test Generation for Validation of Pipelined Processors”, Design Automation and Test in Europe (DATE), 678-683, 2005.
- C9** P. Mishra and N. Dutt, “Functional Validation of Programmable Architectures”, EUROMICRO Symposium on Digital System Design (DSD), pages 12-19, 2005. **[Keynote Paper]**
- C8** P. Mishra and N. Dutt, “Graph-based Functional Test Program Generation for Pipelined Processors”, Design Automation and Test in Europe (DATE), pages 182-187, 2004.
- C7** P. Mishra, A. Kejariwal, and N. Dutt, “Synthesis-driven Exploration of Pipelined Embedded Processors”, International Conference on VLSI Design, pages 921-926, 2004.
- C6** M. Reshadi, P. Mishra, and N. Dutt, “Instruction Set Compiled Simulation: A Technique for Fast and Flexible Instruction Set Simulation”, Design Automation Conference (DAC), pages 758-763, 2003.
- C5** M. Reshadi, N. Bansal, P. Mishra, and N. Dutt, “An Efficient Retargetable Framework for Instruction-Set Simulation”, ACM/IEEE/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), pages 13-18, 2003. **[Best Paper Award]**
- C4** P. Mishra, H. Tomiyama, N. Dutt and A. Nicolau, “Automatic Verification of In-Order Execution in Microprocessors with Fragmented Pipelines and Multicycle Functional Units”, Design Automation and Test in Europe (DATE), pages 36-43, 2002.
- C3** P. Mishra, H. Tomiyama, A. Halambi, P. Grun, N. Dutt and A. Nicolau, “Automatic Modeling and Validation of Pipeline Specifications driven by an Architecture Description Language”, Asia and South Pacific Design Automation Conference (ASPDAC), pages 458-463, 2002.

- C2** P. Mishra, N. Dutt, and A. Nicolau, “*Functional Abstraction driven Design Space Exploration of Heterogeneous Programmable Architectures*”, ACM/IEEE International Symposium on System Synthesis (ISSS), pages 256-261, 2001.
- C1** P. Mishra, P. Grun, N. Dutt, and A. Nicolau, “*Processor-Memory Co-Exploration driven by a Memory-Aware Architecture Description Language*”, International Conference on VLSI Design, 70-75, 2001.

Patents

- P2** Prabhat Mishra, Seok-won Seong, Kanad Basu, Weixun Wang, Xiaoke Qin, *Bitmask-based Code Compression Technique and Decompression Mechanism*, Provisional Patent UF 12654, 2008.
- P1** Prabhat Mishra and Nikil Dutt, *Functional Coverage driven Test Generation for Validation of Pipelined Processors*, United States Patent 7533294, May 12, 2009.

Premier Refereed Workshop Papers with Archival Proceedings

- W10** M. Chen, P. Mishra, and D. Kalita, “*Towards RTL Test Generation from SystemC TLM Specifications*”, IEEE International High Level Design Validation and Test Workshop (HLDVT), November 7-9, 2007.
- W9** H. Koo, P. Mishra, J. Bhadra and M. Abadir, *Directed Micro-architectural Test Generation for an Industrial Processor: A Case Study*, IEEE International Workshop on Microprocessor Test and Verification (MTV), pages -, December 4-5, 2006.
- W8** P. Mishra, H. Koo, and Z. Huang, *Language-driven Validation of Pipelined Processors using Satisfiability Solvers*, IEEE International Workshop on Microprocessor Test and Verification (MTV), 2005.
- W7** P. Mishra, N. Dutt, and Y. Kashai, *Functional Verification of Pipelined Processors: A Case Study*, IEEE International Workshop on Microprocessor Test and Verification (MTV), 2004.
- W6** P. Mishra, A. Kejariwal and N. Dutt, “*Rapid Exploration of Pipelined Processors through Automatic Generation of Synthesizable RTL Models*”, IEEE International Workshop on Rapid System Prototyping (RSP), pages 226-232, 2003.
- W5** P. Mishra and N. Dutt, “*A Methodology for Validation of Microprocessors using Equivalence Checking*”, IEEE International Workshop on Microprocessor Test and Verification, pages 83-88, 2003.
- W4** P. Mishra and N. Dutt, “*Automatic Functional Test Program Generation for Pipelined Processors using Model Checking*”, IEEE International High Level Design Validation and Test Workshop (HLDVT), pages 99-103, 2002.
- W3** P. Mishra, N. Krishnamurthy, N. Dutt, and M. Abadir, “*A Property Checking Approach to Microprocessor Verification using Symbolic Simulation*”, International Workshop on Microprocessor Test and Verification (MTV), 2002.
- W2** P. Mishra, N. Dutt, and A. Nicolau, “*Automatic Validation of Pipeline Specifications*”, IEEE International High Level Design Validation and Test Workshop (HLDVT), pages 9-13, 2001.
- W1** P. Mishra, F. Rousseau, N. Dutt, and A. Nicolau, “*Architecture Description Language driven Design Space Exploration in the Presence of Coprocessors*”, Synthesis And System Integration of Mixed Technologies (SASIMI), 2001.

Magazine Articles

M1 Prabhat Mishra, “*Processor Validation – A Top-Down Approach*”, IEEE Potentials, February-March, pages 29-33, 2005.

PROFESSIONAL SERVICES

Editorial Activity

1. **Guest Editor**, Springer Journal of Electronic Testing (JETTA), *Special Issue on “High-Level Design Validation and Test”*, 2009-2010.
2. **Guest Editor**, Springer International Journal of Parallel Programming (IJPP), *Special Issue on “Nano/Bio-Inspired Applications and Architectures”*, 2008-2009.
3. **Information Director**, ACM Transactions on Design Automation of Electronic Systems, 2004 - 2009.

Organizing Committee

1. **General Chair**, IEEE International High Level Design Validation and Test Workshop, 2010.
2. **Program Chair**, IEEE International High Level Design Validation and Test Workshop, 2009.
3. **Track Chair**, *Synthesis and Verification*, International Conference on VLSI Design, 2009.
4. **Publications Chair**, IEEE International High Level Design Validation and Test Workshop, 2008.

Technical Program Committee

1. Asia and South Pacific Design Automation Conference (ASPDAC), 2010.
2. International Conference on VLSI Design (VLSI Design), 2010.
3. Design Automation and Test in Europe (DATE), 2009.
4. ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2009.
5. International Conference on VLSI Design (VLSI Design), 2009.
6. ACM Great Lakes Symposium on VLSI (GLSVLSI), 2009.
7. IEEE Annual Symposium on VLSI (ISVLSI), 2009.
8. ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2008.
9. International Conference on VLSI Design (VLSI Design), 2008.
10. International Workshop on Constraints in Formal Verification (CFV), 2008.
11. ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis, 2007.
12. International Conference on VLSI Design (VLSI Design), 2007.
13. IEEE International Symposium on Circuits and Systems (ISCAS), 2007.
14. Design Automation and Test in Europe (DATE), 2007.

15. IFIP International Conference on Embedded and Ubiquitous Computing (EUC), 2007.
16. International Symposium on Parallel Architectures, Algorithms, and Networks (I-SPAN), 2007.
17. IEEE International Symposium on Circuits and Systems (ISCAS), 2006.
18. Design Automation and Test in Europe (DATE), 2006.
19. IEEE International Symposium on Circuits and Systems (ISCAS), 2005.

Session Chairs

1. ACM Great Lakes Symposium on VLSI (GLSVLSI), 2009.
2. IEEE International Symposium on VLSI (ISVLSI), 2009.
3. International Conference on VLSI Design (VLSI Design), 2009.
4. ACM/IEEE/IFIP International Conference on Hardware/Software Codesign and System Synthesis, 2008
5. ACM Great Lakes Symposium on VLSI (GLSVLSI), 2008.
6. IEEE International High Level Design Validation and Test Workshop (HLDVT), 2007.
7. IEEE International Workshop on Microprocessor Test and Verification (MTV), 2004
8. IEEE International High Level Design Validation and Test Workshop (HLDVT), 2004.

Reviewer of Scholarly Journals

1. ACM Transactions on Architecture and Code Optimization (TACO)
2. ACM Transactions on Design Automation of Electronic Systems (TODAES)
3. ACM Transactions on Embedded Computing Systems (TECS)
4. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD).
5. IEEE Transactions on Very Large Scale Integration Systems (TVLSI).
6. IEEE Transactions on Computers (Computers)
7. IEEE Transactions on Circuits and Systems II (TCAS-II)
8. IEEE Design and Test of Computers (D&T)
9. Springer Design Automation for Embedded Systems (DAES)
10. Elsevier Journal of Parallel and Distributed Computing (JPDC)
11. Journal on Satisfiability, Boolean Modeling and Computation (JSAT)
12. Elsevier Microelectronics Journal

Offices Held

1. **President**, Indian Graduate Students' Association, University of California, Irvine, 1999.

Reviewer of Premier Conferences

1. IEEE/ACM Design Automation Conference (DAC)
2. IEEE International Conference on Computer-Aided Design (ICCAD)
3. Design Automation and Test in Europe (DATE)
4. Asia and South Pacific Design Automation Conference (ASPDAC)
5. International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES)
6. IEEE International Conference on VLSI Design (VLSI)
7. ACM Great Lakes Symposium on VLSI (GLSVLSI)
8. IEEE Annual Symposium on VLSI (ISVLSI)
9. IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis
10. IEEE Asian Test Symposium (ATS)
11. International SoC Design Conference (ISOCC)
12. IEEE International Symposium on Circuits and Systems (ISCAS)
13. ACM Symposium on Applied Computing (SAC)
14. IEEE International Symposium Pacific Rim Dependable Computing (PRDC)
15. International SoC Design Conference (ISOCC)
16. Workshop on Application Specific Processors (WASP)

Reviewer of Research Proposals

1. NSF Cyber Physical Systems (CPS) Panels, National Science Foundation, 2009.
2. Council of Physical Sciences, Netherlands Organization for Scientific Research (NWO), 2005.

Professional Association Memberships

1. Association for Computing Machinery (ACM), 2004 – 2009.
2. ACM Special Interest Group on Design Automation (SIGDA), 2004 – 2009.
3. **Senior Member**, Institute of Electrical and Electronics Engineers (IEEE), 2000 – 2009.

Invited Seminars and Presentations

1. Indian Institute of Technology (IIT), Kharagpur. Code Compression for Embedded Systems, April 2008.
2. Calcutta University, India. Design Automation of Embedded Systems, December 2006.
3. AMD, Bangalore, India. Functional Validation of Programmable Architectures, Dec 2006.
4. NXP (Philips) Semiconductors, India. Functional Validation of Embedded Systems, Nov 2006.
5. Intel, Bangalore, India. Functional Validation of Programmable Architectures, July 2006.
6. IIT, Kharagpur. Top-Down Validation of Programmable Architectures, June 2005.
7. IIT, Delhi. Language-driven Validation of Embedded Architectures, June 2005.
8. IIT, Kanpur. Specification-driven Validation of Programmable Architectures, June 2005.
9. IIT, Bombay. Top-Down Validation of Programmable Architectures, June 2005.
10. Indian Institute of Science, Bangalore. Validation of Programmable Embedded Architectures, June 2005.
11. Intel, Arizona. Test Generation using Architecture Description Languages, November 2005.

Reviewer of Textbooks

1. Design for Debugging and Validation of Embedded Systems, Morgan Kaufmann, 2008.
2. A Practical Introduction to Hardware/Software Codesign, John Wiley & Sons, 2008.
3. Embedded Systems Debugging and Validation, Morgan Kaufmann, 2007.
4. Embedded Systems: Architecture, Programming and Design, McGraw-Hill, 2005.

Ph.D. ADVISEES (Chair)

1. Heon-Mo Koo, Coverage-directed Test Generation for Validation of Pipelined Processors, Dec 2007.
2. Mingsong Chen, Multicore Verification using Transaction-Level Models, 2006 – 2010 (expected).
3. Weixun Wang, Reconfiguration-Aware Real-Time Scheduling Techniques, 2007 – 2011 (expected).
4. Kanad Basu, Efficient Techniques for Post-silicon Validation and Debug, 2007 – 2012 (expected).
5. Xiaoke Qin, Verification of Dynamic Reconfigurations, 2007 – 2012 (expected).

M.S. ADVISEES (Chair)

1. Seok-won Seong, Dictionary-Based Code Compression Techniques using Bitmasks, March 2006.
2. Chetan Murthy, Decoding-Aware Compression Techniques for Reconfigurable Systems, Dec 2008.
3. Kartik Shrivastava, Integration of Code Compression and Encryption in Embedded Systems, 2010.

UNDERGRADUATE HONORS PROJECT (Chair)

1. David Nash, Use of Similarity in Dictionary Selection for Bitmask-based Code Compression, Dec 2007.

AWARDS AND HONORS FOR STUDENTS

1. Heon-Mo Koo, KUSCO-KSEA Scholarship, Korean-American Scientists and Engineers Association, 2007.
2. Heon-Mo Koo, Korean Graduate Student Research Award, University of Florida, 2006.
3. Kanad Basu, CISE Department Travel Grant, 2008.
4. Mingsong Chen, Young Student Support Program Award, Design Automation Conference, June 2008.
5. Weixun Wang and Xiaoke Qin, DAC University Booth Travel Grant, June 2008.
6. Mingsong Chen, Best Paper Award Nomination, International Conference on VLSI Design, Jan 2009.
7. Weixun Wang, CISE Department Travel Grant, 2009.
8. Xiaoke Qin, DAC Young Student Support Program Award, Design Automation Conference, July 2009.
9. Mingsong Chen, NSF-SRC-SIGDA-DAC Design Automation Summer School, July 2009.

Ph.D. ADVISEES (Committee Member)

1. Pengfei Li, “Synchronization and Control of High Frequency DC-DC Converters”, Dept. of Electrical and Computer Engineering, Proposal Defense – March 03, 2009.

2. Thang N. Dinh, “Detecting Evolving Community Structure in Large and Dynamic Networks”, Department of Computer and Information Science and Engineering, 2008 – 201X
3. Changbum Cho, “Accurate, Scalable and Informative Modeling and Analysis of Complex Workloads and Large-scale Microprocessor Architecture”, Department of Electrical and Computer Engineering, November 24, 2008.
4. Incheol Shin, “Computer Networks”, Department of Computer and Information Science and Engineering, 2008 – 201X.
5. Qiuzhong Wu, “Design of Low-power Digital Circuits, DC-DC Power Converter and Phase-locked Loops”, Department of Electrical and Computer Engineering, 2007– 20XX.
6. Yan Hu, “Modeling and Design for High-Speed Serial Link”, Department of Electrical and Computer Engineering, 2005 – 20XX.
7. John Curreri, Performance Analysis and Verification of Reconfigurable Systems, Department of Electrical and Computer Engineering, 2006 – 2010.
8. Casey Reardon, Abstraction and Simulation for Strategic Design-Space Exploration in Reconfigurable Computing, Department of Electrical and Computer Engineering, 2004 – 2010.
9. Zhe Wang, Department of Computer and Information Science and Engineering, 2008 – 20XX.
10. Duckki Li, Department of Computer and Information Science and Engineering, 2007 – 20XX.
11. Zhuo Huang, Department of Computer and Information Science and Engineering, 2005 – 20XX.
12. Gang Liu, Department of Computer and Information Science and Engineering, 2005 – 20XX.
13. Yi Lin, Department of Computer and Information Science and Engineering, 2005 – 20XX.
14. Daniel Messina, Department of Computer and Information Science and Engineering, June 22, 2007.
15. David Bueno, Department of Electrical and Computer Engineering, January 20, 2006.

M.S. ADVISEES (Committee Member)

1. Udayan Kumar, “Inference of User Behavior and Investigation of Privacy Issues in WLAN Trace Analysis”, Department of Computer and Information Science and Engineering, July 10, 2008.
2. Yilin Shen, Department of Computer and Information Science and Engineering, 2009.
3. Vishal Khanapure, “Memory efficient distributed detection of node replication attacks in wireless sensor networks”, Department of Computer and Information Science and Engineering, July 10, 2009.

UNDERGRADUATE HONORS PROJECT (Committee Member)

1. Bhavya Daya, Rapid Prototyping of Embedded Systems using Field Programmable Gate Arrays, ECE’09

INVITED/REVIEWED RESEARCH DEMONSTRATIONS

1. DAC University Booth, Bitmask-based Code Compression for Embedded Systems, ACM/IEEE Design Automation Conference 2008.

COURSES TAUGHT

Assistant Professor, University of Florida, USA

2004 – 2010: Introduction to Embedded Systems (combined graduate and undergraduate course)

Spring 2005: Computer Architecture Principles (combined graduate and undergraduate course)

2005 – 2009: Hardware Modeling and Verification (graduate-level special topics course)

Assistant Professor, Indian Institute of Science, Bangalore, India

Fall 2006: Embedded Systems: Theory Modeling and Verification (graduate-level course)

UNIVERSITY/DEPARTMENTAL SERVICES

University-Level Services

1. Mentor, University Minority Mentor Program (UMMP), 2008-2010.
2. Mentor, SEAGEP Summer Research Experience for Undergraduates (REU), 2008-2009.

College-Level Services

1. Steering Committee Member, Interdisciplinary Strategic Planning (Energy), 2009–2010

Departmental Services

1. Member, Graduate Admissions Committee, 2005-2010.
2. Member, Scholarships and Awards Committee, 2005-2010.
3. Member, Colloquium Committee, 2007-2010.
4. Commencement Representative, 2004-2006.

RESEARCH FUNDING

	<u>Title</u>	<u>Duration</u>	<u>Agency</u>	<u>Amount</u>	<u>PI/Co-PI</u>
1.	NSF CAREER (functional verification)	06/2008 – 05/2013	NSF	\$400,000	PI (100%)
2.	Multi-core Chip Design & Architecture	08/2009 – 07/2012	NSF+SRC	\$300,000	Co-PI (40%)
3.	NSF CSR (compression and encryption)	08/2009 – 07/2011	NSF	\$100,000	PI (100%)
4.	Transaction-Level SOC Validation	11/2006 – 08/2009	Intel	\$120,000	PI (100%)
5.	Equipment/SW Donation	September 2007	Xilinx	\$10,000	PI (100%)
6.	Equipment/SW Donation	February 2005	Altera	\$3,000	PI (100%)