

CURRICULUM VITAE

Prabhat Mishra

Associate Professor

*Dept. of Computer and Information Science and Engineering
University of Florida, Gainesville, FL 32611-6120, USA*

Tel: (352) 505 1880

Fax: (352) 392 1220

Email: prabhat@cise.ufl.edu

URL: <http://www.cise.ufl.edu/~prabhat>

RESEARCH INTERESTS: Design automation for embedded and reconfigurable systems, VLSI CAD, hardware/software verification using a combination of simulation-based techniques and formal methods.

EDUCATION

Ph.D.	Information and Computer Science	University of California , Irvine, USA	2004
M.Tech.	Computer and Information Technology	Indian Institute of Technology , Kharagpur	1996
B.E.	Computer Science and Engineering	Jadavpur University , Kolkata, India	1994

EMPLOYMENT

Since Aug 16, 2010	<i>Associate Professor</i>	CISE, University of Florida , Gainesville, USA
Jul 2004 – Aug 2010	<i>Assistant Professor</i>	CISE, University of Florida , Gainesville, USA
May 2006 – Dec 2006	<i>Assistant Professor</i>	Indian Institute of Science , Bangalore, India
Apr 2004 – Jul 2004	<i>Assistant Project Scientist</i>	CECS, University of California , Irvine, USA
Jul 1999– Mar 2004	<i>Research/Teaching Assistant</i>	University of California , Irvine, USA
Summer 2001, 2002	<i>Research Intern</i>	Motorola (Freescale), Austin, Texas, USA
Summer 2000	<i>Research Intern</i>	Intel , Santa Clara, California, USA
Dec 1998 – Jun 1999	<i>Senior R&D Engineer</i>	Synopsys , Bangalore, India
Jul 1997 – Dec 1998	<i>Senior Software Engineer</i>	Silicon Automation Systems , Bangalore, India
Feb 1996 – Jun 1997	<i>Software Design Engineer</i>	Texas Instruments , Bangalore, India

AWARDS / ACHIEVEMENTS

1. **Best Paper Award**, International Conference on VLSI Design, January 2011.
2. **NSF CAREER Award**, National Science Foundation, 2008 – 2013.
3. **Best Paper Award Nominations**, DATE 2012 and DAC 2009.
4. **International Educator of the Year Award**, College of Engineering, University of Florida, 2007.
5. **EDAA Outstanding Dissertation Award**, European Design and Automation Association, 2004.
6. **Best Paper Award**, ACM/IEEE CODES+ISSS Conference, October 2003.
7. **Senior Member** of ACM; **Senior Member** of IEEE.

SUMMARY OF PUBLICATIONS

- 4 Books (Springer'12, Springer'11, Morgan Kaufmann'08 and Springer'05), 10 book chapters and 2 patents
- 28 journal articles, 48 referred conference papers, 10 referred workshop papers with archival proceedings

SUMMARY OF PROFESSIONAL SERVICES

- **Associate Editor** (ACM TODAES, IEEE Design & Test, JETTA), **Guest Editor** (IEEE Trans. Computers)
- **General Chair** (HLDVT'10), **Track Chair** (CODES+ISSS, IC3 and VLSI), **Program Chair** (HLDVT'09)
- **Technical Program Committee** (ICCAD, DATE, ASPDAC, CODES+ISSS, VLSI Design, and ISCAS)

SELECTED PUBLICATIONS

Books

- B4** M. Chen, X. Qin and P. Mishra, System-Level Validation: High-Level Modeling and Directed Test Generation Techniques, **Springer**, to appear in late 2012.
- B3** W. Wang, P. Mishra and S. Ranka, *Dynamic Reconfiguration in Real-Time Systems - Energy, Performance, Reliability and Thermal Perspectives*, **Springer**, to appear in early 2012.
- B2** P. Mishra and N. Dutt, “*Functional Verification of Programmable Embedded Architectures: A Top-Down Approach*”, **Springer**, ISBN 0-387-26143-5, July 2005.
- B1** P. Mishra and N. Dutt, Editors, “*Processor Description Languages: Applications and Methodologies*”, ISBN 978-0-12-3742872, **Morgan Kaufmann**, June 2008.

Journal Articles

- J28** K. Basu and P. Mishra, Restoration-Aware Trace Signal Selection for Post Silicon Validation, Accepted to appear in IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI), 2012.
- J27** X. Qin, W. Wang and P. Mishra, TCEC: Temperature- and Energy-Constrained Scheduling in Real-Time Multitasking Systems, Accepted to appear in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2012.
- J26** K. Basu, C. Murthy and P. Mishra, Bitmask aware Compression of NISC Control Words, Elsevier Integration, the VLSI Journal (INTEGRATION), 2012. DOI: 10.1016/j.vlsi.2012.02.004
- J25** X. Qin and P. Mishra, Directed Test Generation for Validation of Multicore Architectures, Accepted to appear in ACM Transactions on Design Automation of Electronic Systems (TODAES), 2012.
- J24** H. Hajimiri, K. Rahmani and P. Mishra, Compression-Aware Dynamic Cache Reconfiguration for Embedded Systems, To appear in Elsevier Sustainable Computing: Informatics and Systems, 2012.
- J23** W. Wang, P. Mishra and A. Gordon-Ross, *Dynamic Cache Reconfiguration for Soft Real-Time Systems*, Accepted to appear in ACM Transactions on Embedded Computing Systems (TECS), 2011.
- J22** M. Chen, P. Mishra and D. Kalita, *Automatic RTL Test Generation from SystemC TLM Specifications*, Accepted to appear in ACM Transactions on Embedded Computing Systems (TECS), 2011.
- J21** M. Chen and P. Mishra, *Property Learning Techniques for Efficient Generation of Directed Tests*, Accepted to appear in IEEE Transactions on Computers (TC), 2011.
- J20** W. Wang and P. Mishra, *System-Wide Leakage-Aware Energy Minimization using Dynamic Voltage Scaling and Cache Reconfiguration in Multitasking Systems*, Accepted to appear in IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI), 2011.
- J19** W. Wang and P. Mishra, *Dynamic Reconfiguration of Two-Level Cache Hierarchy in Real-Time Embedded Systems*, Accepted to appear in Journal of Low Power Electronics (JOLPE), 2011.
- J18** W. Wang, S. Ranka and P. Mishra, *Energy-Aware Dynamic Reconfiguration Algorithms for Real-Time Multitasking Systems*, Elsevier Sustainable Computing: Informatics and Systems(SUSCOM), 2010.

- J17** M. Chen, P. Mishra and D. Kalita, *Efficient Test Case Generation for Validation of UML Activity Diagrams*, Accepted to appear in Springer Design Automation for Embedded Systems (DAES), 2010.
- J16** M. Chen and P. Mishra, *Efficient Techniques for Directed Test Generation using Incremental Satisfiability*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2009.
- J15** X. Qin, C. Murthy and P. Mishra, Decoding-aware Compression of FPGA Bitstreams, Accepted to appear in IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI), 2009.
- J14** K. Basu and P. Mishra, “*Test-Data Compression using Application-Aware Bitmask and Dictionary Selection Methods*”, IEEE Transactions on Very Large Scale Integration Systems (TVLSI), volume 18, issue 9, pages 1277-1286, 2010. DOI: 10.1109/TVLSI.2009.2024116.
- J13** X. Qin and P. Mishra, *A Universal Placement Technique of Compressed Instructions for Efficient Parallel Decompression*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), volume 28, no 8, pages 1224-1236, August 2009.
- J12** H. Koo and P. Mishra, Functional Test Generation using Design and Property Decomposition Techniques, ACM Transactions on Embedded Computing Systems (TECS), vol 8, no 4, article 32, July 2009.
- J11** S. Seong and P. Mishra, *Bitmask-Based Code Compression for Embedded Systems*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 27(4), pages 673-685, 2008.
- J10** P. Mishra and N. Dutt, *Specification-driven Directed Test Generation for Validation of Pipelined Processors*, ACM Transactions on Design Automation of Electronic Systems (TODAES), volume 13, no 3, 36 pages, Article 42, July 2008.
- J9** M. Reshadi, P. Mishra and N. Dutt, “*Hybrid Compiled Simulation: An Efficient Technique for Instruction-Set Architecture Simulation*”, ACM Transactions on Embedded Computing Systems (TECS), volume 8, no 3, April 2009.
- J8** P. Mishra, A. Shrivastava and N. Dutt, “*Architecture Description Language (ADL)-driven Software Toolkit Generation for Architectural Exploration of Programmable SOCs*”, ACM Transactions on Design Automation of Electronic Systems (TODAES), volume 11, no 3, pages 1-33, July 2006.
- J7** M. Reshadi, P. Mishra and N. Dutt, “*A Retargetable Framework for Instruction-Set Architecture Simulation*”, ACM Transactions on Embedded Computing Systems (TECS), 5(2), pages 431-452, 2006.
- J6** P. Mishra and N. Dutt, “*Architecture Description Languages for Programmable Embedded Systems*”, IEE Proceedings on Computers and Digital Techniques (CDT), 152(3), pages 285-297, May 2005.
- J5** P. Mishra, N. Dutt, N. Krishnamurthy and M. Abadir, “*A Methodology for Validation of Microprocessors using Symbolic Simulation*”, Inderscience International Journal of Embedded Systems (IJES), 1(1/2), pages 14-22, 2005.
- J4** P. Mishra, N. Dutt, N. Krishnamurthy, and M. Abadir, “*A Top-Down Methodology for Validation of Microprocessors*”, IEEE Design & Test of Computers, 21(2), pages 122-131, March-April, 2004.
- J3** P. Mishra, N. Dutt, and H. Tomiyama, “*Towards Automatic Validation of Dynamic Behavior in Pipelined Processor Specifications*”, Kluwer Design Automation for Embedded Systems (DAES), 8(2), pages 249-265, 2003.

- J2** P. Mishra and N. Dutt, “*Modeling and Validation of Pipeline Specifications*”, ACM Transactions on Embedded Computing Systems (TECS), 3(1), pages 140-162, 2004.
- J1** P. Mishra, M. Mamidipaka, and N. Dutt, “*Processor-Memory Co-Exploration using an Architecture Description Language*”, ACM Transactions on Embedded Computing Systems (TECS), 3(1), pages 114-139, 2004.

Book Chapters

- BC10** P. Mishra, *Computer Architecture*, Encyclopedia of Life Support Systems (EOLSS), United Nations Educational, Scientific and Cultural Organization (UNESCO), 2012
- BC9** W. Wang, X. Qin and P. Mishra, “*Energy-Aware Dynamic Cache Reconfigurations and Voltage Scaling in Real-Time Systems*”, Handbook of Energy-Aware and Green Computing, I. Ahmad and S. Ranka, Editors, Chapman & Hall/CRC Press, 2011.
- BC8** N. Bandyopadhyay, K. Basu and P. Mishra, “*HMDDES, ISDL and other Contemporary ADLs*”, in *Processor Description Languages: Applications and Methodologies*, Prabhat Mishra and Nikil Dutt, Editors, Morgan Kaufmann Publishers, 2008.
- BC7** P. Mishra and A. Shrivastava, “*ADL-driven Methodologies for Design Automation of Embedded Processors*”, in *Processor Description Languages: Applications and Methodologies*, Prabhat Mishra and Nikil Dutt, Editors, Morgan Kaufmann Publishers, 2008.
- BC6** P. Mishra and N. Dutt, “*EXPRESSION: An ADL for Software Toolkit Generation, Exploration, and Validation of Programmable SOC Architectures*”, in *Processor Description Languages: Applications and Methodologies*, Prabhat Mishra and Nikil Dutt, Editors, Morgan Kaufmann Publishers, 2008.
- BC5** P. Mishra and N. Dutt, “*Introduction to Architecture Description Languages*”, in *Processor Description Languages: Applications and Methodologies*, Prabhat Mishra and Nikil Dutt, Editors, Morgan Kaufmann Publishers, 2008.
- BC4** P. Mishra and N. Dutt, “*Architecture Description Languages*”, in *Customizable and Configurable Embedded Processors*”, Paolo Ienne and Rainer Leupers, Editors, Morgan Kaufmann, 2006.
- BC3** P. Mishra and N. Dutt, “*Processor Modeling and Design Tools*”, in *The EDA Handbook*, G. Martin, L. Lavagno, and L. Scheffer, Editors, CRC Press, 2005.
- BC2** P. Mishra and N. Dutt, “*Architecture Description Languages for Programmable Embedded Systems*”, in *SOC: Next Generation Electronics*, Bashir M. Al-Hashimi, Editor, IEE Press, 2005.
- BC1** P. Mishra and N. Dutt, “*Modeling and Verification of Pipelined Embedded Processors in the Presence of Hazards and Exceptions*”, in *Design and Analysis of Distributed Embedded Systems*, Kluwer Academic Publishers, pages 81-90, 2002.

Referred Conference Papers

- C48** K. Rahmani, H. Hajimiri, K. Shrivastava and P. Mishra, Synergistic Integration of Code Encryption and Compression in Embedded Systems, ACM Great Lakes Symposium on VLSI (GLSVLSI), 2012.

- C47** K. Rahmani, P. Mishra and S. Bhunia, Memory-based Computing for Performance and Energy Improvement in Multicore Architectures, ACM Great Lakes Symposium on VLSI (GLSVLSI), 2012.
- C46** X. Qin and P. Mishra, Automated Generation of Directed Tests for Transition Coverage in Cache Coherence Protocols, Design Automation and Test in Europe (DATE), 2012. **[Nominated for Best Paper Award]**
- C45** H. Hajimiri and P. Mishra, Intra-task Dynamic Cache Reconfiguration, International Conference on VLSI Design, pages -, 2012.
- C44** Z. Wang, S. Ranka and P. Mishra, *Temperature-aware Task Partitioning for Real-Time Scheduling in Embedded Systems*, International Conference on VLSI Design, pages -, 2012.
- C43** K. Basu, P. Mishra and P. Patra, *Efficient Combination of Trace and Scan Signals for Post Silicon Validation and Debug*, IEEE International Test Conference (ITC), pages - , 2011.
- C42** W. Wang, P. Mishra and S. Ranka, *Dynamic Cache Reconfiguration and Partitioning for Energy Optimization in Real-Time Multi-Core Systems*, Accepted to appear in ACM/IEEE Design Automation Conference (DAC), pages - , 2011.
- C41** H. Hajimiri, K. Rahmani, and P. Mishra, *Synergistic Integration of Dynamic Cache Reconfiguration and Code Compression in Embedded Systems*, International Green Computing Conference (IGCC), 2011.
- C40** H. Hajimiri, S. Paul, A. Ghosh, S. Bhunia and P. Mishra, *Reliability Improvement in Multicore Architectures Through Computing in Embedded Memory*, IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), pages , 2011.
- C39** X. Qin and P. Mishra, “*Efficient Directed Test Generation for Validation of Multicore Architectures*”, Accepted to appear in International Symposium on Quality Electronic Design (ISQED), pages -, 2011.
- C38** K. Basu and P. Mishra, *Efficient Trace Data Compression using Statically Selected Dictionary*, Accepted to appear in IEEE VLSI Test Symposium (VTS), pages -, 2011.
- C37** M. Chen and P. Mishra, *Decision Ordering Based Property Decomposition for Functional Test Generation*, Accepted to appear in Design Automation and Test in Europe (DATE), pages -, 2011.
- C36** K. Basu and P. Mishra, *Efficient Trace Signal Selection for Post Silicon Validation and Debug*, International Conference on VLSI Design, pages 352-357, 2011. **[Best Paper Award]**
- C35** K. Shrivastava and P. Mishra, *Dual Code Compression for Embedded Systems*, International Conference on VLSI Design, pages 177-182, 2011.
- C34** W. Wang, S. Ranka and P. Mishra, *A General Algorithm for Energy-Aware Dynamic Reconfiguration in Multitasking Systems*, International Conference on VLSI Design, pages -, 2011.
- C33** W. Wang and P. Mishra, Pre-DVS: Preemptive Dynamic Voltage Scaling for Real-Time Systems with Approximation Scheme, ACM/IEEE Design Automation Conference (DAC), pages-, 2010.
- C32** W. Wang, X. Qin and P. Mishra, *Temperature- and Energy-Constrained Scheduling in Multitasking Systems: A Model Checking Approach*, ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), pages -, 2010.

- C31** M. Chen, X. Qin and P. Mishra, *Efficient Decision Ordering Techniques for SAT-based Test Generation*, Design Automation and Test in Europe (DATE), pages 490-495, 2010.
- C30** X. Qin, M. Chen and P. Mishra, *Synchronized Generation of Directed Tests using Satisfiability Solving*, International Conference on VLSI Design, pages -, 2010.
- C29** W. Wang and P. Mishra, *Leakage-Aware Energy Minimization using Dynamic Voltage Scaling and Cache Reconfiguration in Real-Time Systems*, International Conference on VLSI Design, pages -, 2010.
- C28** N. Dang, A. Roychoudhury, T. Mitra and P. Mishra, *“Generating Test Programs to Cover Pipeline Interactions”*, Design Automation Conference (DAC), 142-147, 2009. **[Best Paper Award Nomination]**
- C27** W. Wang and P. Mishra, *“Dynamic Reconfiguration of Two-Level Caches in Soft Real-Time Embedded Systems”*, IEEE International Symposium on VLSI (ISVLSI), pages -, 2009.
- C26** C. Murthy and P. Mishra, *“Lossless Compression using Efficient Encoding of Bitmasks”*, IEEE International Symposium on VLSI (ISVLSI), pages -, 2009.
- C25** C. Murthy and P. Mishra, *“Bitmask-based Control Word Compression for NISC Architecture”*, ACM Great Lakes Symposium on VLSI (GLSVLSI), pages -, 2009.
- C24** X. Qin and P. Mishra, *“Efficient Placement of Compressed Code for Parallel Decompression”*, International Conference on VLSI Design, pages 335–340, 2009.
- C23** W. Wang, P. Mishra and Ann Gordon-Ross, *“SACR: Scheduling-Aware Cache Reconfiguration for Real-Time Embedded Systems”*, International Conference on VLSI Design, pages 547–552, 2009.
- C22** P. Mishra and M. Chen, *“Efficient Techniques for Directed Test Generation using Incremental Satisfiability”*, International Conference on VLSI Design, 65–70, 2009. **[Best Paper Award Nomination]**
- C21** H-M. Koo and P. Mishra, *“Specification-based Compaction of Directed Tests for Functional Validation of Pipelined Processors”*, ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), pages 137–142, 2008.
- C20** K. Basu and P. Mishra, *“A Novel Test-Data Compression Technique using Application-Aware Bitmask and Dictionary Selection Methods”*, ACM Great Lakes Symposium on VLSI (GLSVLSI), 83–88, 2008.
- C19** M. Chen and P. Mishra, *“Coverage-driven Automatic Test Generation for UML Activity Diagrams”*, ACM Great Lakes Symposium on VLSI (GLSVLSI), pages 139–142, Orlando, May 4 – 6, 2008.
- C18** S. Seong and P. Mishra, *“An Efficient Code Compression Technique using Application-Aware Bitmask and Dictionary Selection Methods”*, Design Automation and Test in Europe (DATE), 582 – 587, 2007.
- C17** H-M. Koo and P. Mishra, *“Automated Micro-architectural Test Generation for Validation of Modern Processors”*, US-Korea Conference on Global Challenges in Science and Technology (UKC), Washington DC, August 9-12, 2007.
- C16** X. Li, A. Roychoudhury, T. Mitra, P. Mishra and X. Cheng, *“A Retargetable Software Timing Analyzer Using Architecture Description Language”*, Asia and South Pacific Design Automation Conference (ASPDAC), pages 396-401, 2007.
- C15** S. Seong and P. Mishra, *“A Bitmask-based Code Compression Technique for Embedded Systems”*, IEEE/ACM International Conference on Computer Aided Design (ICCAD), pages 251 – 254, 2006.

- C14** H. Koo and P. Mishra, “*Test Generation using SAT-based Bounded Model Checking for Validation of Pipelined Processors*”, ACM Great Lakes Symposium on VLSI (GLSVLSI), pages 362-365, 2006.
- C13** H. Koo and P. Mishra, “*Coverage-driven Functional Test Generation for Processor Validation using Formal Methods*”, US-Korea Conference on Science, Technology, and Entrepreneurship (UKC), 2006.
- C12** H. Koo and P. Mishra, “*Functional Test Generation using Property Decompositions for Validation of Pipelined Processors*”, Design Automation and Test in Europe (DATE), pages 1240-1245, 2006.
- C11** M. Reshadi and P. Mishra, “*Memory Access Optimizations in Instruction-Set Simulators*”, International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), pages 237-242, 2005.
- C10** P. Mishra and N. Dutt, “*Functional Coverage Driven Test Generation for Validation of Pipelined Processors*”, Design Automation and Test in Europe (DATE), 678-683, 2005.
- C9** P. Mishra and N. Dutt, “*Functional Validation of Programmable Architectures*”, EUROMICRO Symposium on Digital System Design (DSD), pages 12-19, 2005. **[Keynote Paper]**
- C8** P. Mishra and N. Dutt, “*Graph-based Functional Test Program Generation for Pipelined Processors*”, Design Automation and Test in Europe (DATE), pages 182-187, 2004.
- C7** P. Mishra, A. Kejariwal, and N. Dutt, “*Synthesis-driven Exploration of Pipelined Embedded Processors*”, International Conference on VLSI Design, pages 921-926, 2004.
- C6** M. Reshadi, P. Mishra, and N. Dutt, “*Instruction Set Compiled Simulation: A Technique for Fast and Flexible Instruction Set Simulation*”, Design Automation Conference (DAC), pages 758-763, 2003.
- C5** M. Reshadi, N. Bansal, P. Mishra, and N. Dutt, “*An Efficient Retargetable Framework for Instruction-Set Simulation*”, ACM/IEEE/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), pages 13-18, 2003. **[Best Paper Award]**
- C4** P. Mishra, H. Tomiyama, N. Dutt and A. Nicolau, “*Automatic Verification of In-Order Execution in Microprocessors with Fragmented Pipelines and Multicycle Functional Units*”, Design Automation and Test in Europe (DATE), pages 36-43, 2002.
- C3** P. Mishra, H. Tomiyama, A. Halambi, P. Grun, N. Dutt and A. Nicolau, “*Automatic Modeling and Validation of Pipeline Specifications driven by an Architecture Description Language*”, Asia and South Pacific Design Automation Conference (ASPDAC), pages 458-463, 2002.
- C2** P. Mishra, N. Dutt, and A. Nicolau, “*Functional Abstraction driven Design Space Exploration of Heterogeneous Programmable Architectures*”, ACM/IEEE International Symposium on System Synthesis (ISSS), pages 256-261, 2001.
- C1** P. Mishra, P. Grun, N. Dutt, and A. Nicolau, “*Processor-Memory Co-Exploration driven by a Memory-Aware Architecture Description Language*”, International Conference on VLSI Design, pages 70-75, 2001.

Patents

- P2** Prabhat Mishra, Seok-won Seong, Kanad Basu, Weixun Wang, Xiaoke Qin, *Bitmask-based Code Compression Technique and Decompression Mechanism*, Provisional Patent UF 12654, 2007.
- P1** Prabhat Mishra and Nikil Dutt, *Functional Coverage driven Test Generation for Validation of Pipelined Processors*, United States Patent 7533294, May 12, 2009.

Premier Refereed Workshop Papers with Proceedings

- W10** M. Chen, P. Mishra, and D. Kalita, “Towards RTL Test Generation from SystemC TLM Specifications”, IEEE International High Level Design Validation and Test Workshop (HLDVT), November 7-9, 2007.
- W9** H. Koo, P. Mishra, J. Bhadra and M. Abadir, Directed Micro-architectural Test Generation for an Industrial Processor: A Case Study, IEEE International Workshop on Microprocessor Test and Verification (MTV), pages -, December 4-5, 2006.
- W8** P. Mishra, H. Koo, and Z. Huang, *Language-driven Validation of Pipelined Processors using Satisfiability Solvers*, IEEE International Workshop on Microprocessor Test and Verification (MTV), 2005.
- W7** P. Mishra, N. Dutt, and Y. Kashai, *Functional Verification of Pipelined Processors: A Case Study*, IEEE International Workshop on Microprocessor Test and Verification (MTV), 2004.
- W6** P. Mishra, A. Kejariwal and N. Dutt, “Rapid Exploration of Pipelined Processors through Automatic Generation of Synthesizable RTL Models”, IEEE International Workshop on Rapid System Prototyping (RSP), pages 226-232, 2003.
- W5** P. Mishra and N. Dutt, “A Methodology for Validation of Microprocessors using Equivalence Checking”, IEEE International Workshop on Microprocessor Test and Verification, pages 83-88, 2003.
- W4** P. Mishra and N. Dutt, “Automatic Functional Test Program Generation for Pipelined Processors using Model Checking”, International High Level Design Validation and Test Workshop, 99-103, 2002.
- W3** P. Mishra, N. Krishnamurthy, N. Dutt, and M. Abadir, “A Property Checking Approach to Microprocessor Verification using Symbolic Simulation”, IEEE International Workshop on Microprocessor Test and Verification (MTV), 2002.
- W2** P. Mishra, N. Dutt, and A. Nicolau, “Automatic Validation of Pipeline Specifications”, IEEE International High Level Design Validation and Test Workshop (HLDVT), pages 9-13, 2001.
- W1** P. Mishra, F. Rousseau, N. Dutt, and A. Nicolau, “Architecture Description Language driven Design Space Exploration in the Presence of Coprocessors”, Synthesis And System Integration of MIXed Technologies (SASIMI), 2001.

Non-Referred Publications (Magazine Articles, Guest Editorials, etc.)

- M6** Prabhat Mishra, Zeljko Zilic and Sandeep Shukla, Guest Editors' Introduction: Multicore SoC Validation with Transaction-Level Models, IEEE Design & Test of Computers, May/June 2011.
- M5** Sandeep Shukla, Prabhat Mishra and Zeljko Zilic, A Brief History of Multiprocessors and EDA, IEEE Design & Test of Computers, May/June 2011.
- M4** Zeljko Zilic, Prabhat Mishra and Sandeep Shukla, Challenges of Rapidly Emerging Consumer Space Multiprocessors, IEEE Design & Test of Computers, May/June 2011.
- M3** Prabhat Mishra, Guest Editorial, Journal of Electronic Testing, volume 26, number 2, pages 149-150, 2010.
- M2** Prabhat Mishra, Guest Editor Introduction: Special Issue on Nano/Bio-Inspired Applications and Architectures, International Journal of Parallel Programming, volume 37, number 4, pages 343-344, 2009.
- M1** P. Mishra, “Processor Validation - A Top-Down Approach”, IEEE Potentials, February-March, 29-33, 2005.

PROFESSIONAL SERVICES

Editorial Activity

1. **Associate Editor**, ACM Transactions on Design Automation of Electronic Systems, 2012-2013.
2. **Associate Editor**, IEEE Design & Test of Computers, *Embedded Real-Time Systems*, 2011-2013.
3. **Associate Editor**, Springer Journal of Electronic Testing (JETTA), 2012-2013.
4. **Guest Editor**, IEEE Transactions on Computers, *Special Issue on "Transaction-Level Validation of Multicore Architectures"*, 2010-2011.
5. **Guest Editor**, IEEE Design & Test of Computers, *Special Issue on "System-Level Design & Validation of Heterogeneous Chip Multiprocessors"*, 2011-2012.
6. **Guest Editor**, Springer Journal of Electronic Testing (JETTA), *Special Issue on "High-Level Design Validation and Test"*, 2009-2010.
7. **Guest Editor**, Springer International Journal of Parallel Programming (IJPP), *Special Issue on "Nano/Bio-Inspired Applications and Architectures"*, 2008-2009.
8. **Information Director**, ACM Transactions on Design Automation of Electronic Systems, 2004 - 2010.

Organizing Committee

1. **General Chair**, IEEE International High Level Design Validation and Test Workshop, 2010.
2. **Program Chair**, IEEE International High Level Design Validation and Test Workshop, 2009.
3. **Track Chair**, *Application-Specific Architectures and Algorithms*, ACM/IEEE International Conference on Hardware-Software Co-Design and System Synthesis (CODES+ISSS), 2010.
4. **Track Chair**, *Verification, testing, pre- and post-silicon validation, failure analysis*, ACM/SIGDA Ph.D. Forum at DAC, 2010.
5. **Track Chair**, *Systems*, International Conference on Contemporary Computing (IC3), 2010.
6. **Track Chair**, *Synthesis and Verification*, International Conference on VLSI Design, 2009.
7. **Publications Chair**, IEEE International High Level Design Validation and Test Workshop, 2008.

Technical Program Committee

1. International Conference on Computer-Aided Design (ICCAD), 2011
2. Asia and South Pacific Design Automation Conference (ASPDAC), 2010 – 2011.
3. International Symposium on VLSI Design, Automation and Test (VLSI-DAT), 2011.
4. International Conf. on Hardware/Software Codesign and System Synthesis (CODES+ISSS), 2007– 2011
5. International Conference on VLSI Design (VLSI Design), 2007 – 2011.
6. Design Automation and Test in Europe (DATE), 2006 – 2010.
7. ACM Great Lakes Symposium on VLSI (GLSVLSI), 2009 – 2010, 2012.
8. IEEE Annual Symposium on VLSI (ISVLSI), 2009 – 2010.
9. IEEE/IFIP International Conference on VLSI and System-on-Chip (VLSI-SoC), 2010.
10. IEEE International Symposium on Circuits and Systems (ISCAS), 2005 – 2007.
11. IFIP International Conference on Embedded and Ubiquitous Computing (EUC), 2007.
12. International Symposium on Parallel Architectures, Algorithms, and Networks (I-SPAN), 2007.

Session Chairs

1. International Conference on VLSI Design (VLSI Design), 2009, 2011, 2012.
2. ACM Great Lakes Symposium on VLSI (GLSVLSI), 2008, 2009.
3. IEEE International Symposium on VLSI (ISVLSI), 2009.
4. ACM/IEEE/IFIP International Conference on Hardware/Software Codesign and System Synthesis, 2008
5. IEEE International Workshop on Microprocessor Test and Verification (MTV), 2004
6. IEEE International High Level Design Validation and Test Workshop (HLDVT), 2004, 2007.

Reviewer of Scholarly Journals

1. ACM Transactions on Architecture and Code Optimization (TACO), 2004 – 2007.
2. ACM Transactions on Design Automation of Electronic Systems (TODAES), 2004 – 2008.
3. IEEE Design and Test of Computers (D&T), 2004 – 2010.
4. ACM Transactions on Embedded Computing Systems (TECS), 2004 – 2008.
5. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD).
6. IEEE Transactions on Very Large Scale Integration Systems (TVLSI).
7. IEEE Transactions on Computers (Computers), 2005 – 2007.
8. IEEE Transactions on Circuits and Systems II (TCAS-II), 2005 – 2007.
9. Springer Design Automation for Embedded Systems (DAES), 2004 – 2007.
10. Elsevier Journal of Parallel and Distributed Computing (JPDC), 2008.
11. Journal on Satisfiability, Boolean Modeling and Computation (JSAT), 2007.

Reviewer of Premier Conferences

1. IEEE/ACM Design Automation Conference (DAC), 2000 – 2010.
2. IEEE International Test Conference (ITC), 2010.
3. IEEE International Conference on Computer-Aided Design (ICCAD), 2000 – 2007.
4. Design Automation and Test in Europe (DATE), 2000 – 2007.
5. Asia and South Pacific Design Automation Conference (ASPDAC), 2000 – 2007, 2010.
6. International Conference on Compilers, Architectures, and Synthesis for Embedded Systems, 2000 – 2007.
7. IEEE International Conference on VLSI Design (VLSI), 2000 – 2007.
8. ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis, 2000 – 2007.
9. IEEE Asian Test Symposium (ATS), 2005.
10. IEEE International Symposium on Circuits and Systems (ISCAS), 2004 – 2007.

Reviewer of Research Proposals

1. Deanship of Scientific Research, King Fahd University of Petroleum and Minerals, 2010, 2011.
2. NSF Computer Systems Research (CSR) Panel, National Science Foundation, 2010.
3. NSF Cyber Physical Systems (CPS) Panels, National Science Foundation, 2009.
4. Council of Physical Sciences, Netherlands Organization for Scientific Research (NWO), 2005.

Offices Held

1. **President**, Indian Graduate Students' Association, University of California, Irvine, 1999.

Professional Association Memberships

1. **Senior Member**, Association for Computing Machinery (ACM), 2010.
2. **Senior Member**, Institute of Electrical and Electronics Engineers (IEEE), 2008 – 2010.
3. ACM Special Interest Group on Design Automation (SIGDA), 2004 - 2010.

Ph.D. ADVISEES (Chair)

1. Heon-Mo Koo, Coverage-directed Test Generation for Validation of Pipelined Processors, December 2007. **Employment:** Intel Corporation, Folsom, California, USA.
2. Mingsong Chen, Efficient Approaches for Functional Validation of SoC Designs using High-Level Specifications, August 2010. **Employment:** *Associate Professor*, East China Normal University, China.
3. Weixun Wang, Energy-Aware Scheduling and Dynamic Reconfiguration in Real-Time Embedded Systems, August 2011. **Employment:** Amazon, USA.
4. Xiaoke Qin, System-Level Validation of Multicore Architectures, May 2012. **Employment:** Microsoft USA
5. Kanad Basu, Efficient Techniques for Post-silicon Validation and Debug, 2007 – 2012 (expected).
6. Hadi Hajimiri, Memory-based Computing, 2008 – 2013 (expected).
7. Kamran Rahmani, Embedded Systems Security, 2009 – 2014 (expected).

AWARDS AND HONORS FOR STUDENTS

1. **Heon-Mo Koo** (Ph.D., 2007)
 - KUSCO-KSEA Scholarship from the Korean-American Scientists and Engineers Association, 2007.
 - Korean Graduate Student Research Award from the University of Florida, 2006.
2. **Mingsong Chen** (Ph.D., 2010)
 - ACM/SIGDA Ph.D. Forum at DAC, Design Automation Conference, June 2010.
 - **Best Paper Award Nomination**, International Conference on VLSI Design, Jan 2009.
 - DAC Young Student Support Program Award, Design Automation Conference, June 2008.
3. **Weixun Wang** (Ph.D., 2011)
 - ACM SIGDA Ph.D. Forum at DAC, Design Automation Conference, June 2011.
4. **Xiaoke Qin** (Ph.D., 2012)
 - **Best Paper Award Nomination**, Design Automation and Test in Europe (DATE), 2012.
 - DAC Young Student Support Program Award, Design Automation Conference, July 2009.
5. **Kanad Basu** (Ph.D. Student)
 - **Best Paper Award**, International Conference on VLSI Design, 2011.
6. **Hadi Hajimiri** (Ph.D. Student)
 - DAC Young Student Support Program Award, Design Automation Conference, July 2011.

M.S. ADVISEES (Chair)

1. Seok-won Seong, Dictionary-Based Code Compression Techniques using Bitmasks for Embedded Systems, March 2006. **Employment:** *Senior Engineer*, Turn Inc, USA.
2. Chetan Murthy, Decoding-Aware Compression Techniques for Reconfigurable Systems, December 2008. **Employment:** *Member Technical Staff*, Juniper Networks, USA.
3. Kartik Shrivastava, Synergistic Integration of Code Compression and Encryption in Embedded Systems, August 2010. **Employment:** *ASIC Engineer*, NVIDIA, Bangalore, India.

COURSES TAUGHT

University of Florida, USA

- Spring 2012:** Computer Architecture (graduate core course)
- Fall 2011:** Embedded Systems (combined graduate and undergraduate course)
- Spring 2011:** Introduction to Computer Organization (undergraduate course)
- Fall 2004-2010:** Computer Architecture (combined graduate core course and undergraduate elective)
- Spring 2005-2010:** Embedded Systems (combined graduate and undergraduate course)
- Fall 2005:** Hardware Modeling and Verification (graduate-level special topics course)

Indian Institute of Science, Bangalore, India

- Fall 2006:** Embedded Systems: Theory Modeling and Verification (graduate-level course)

UNIVERSITY/DEPARTMENTAL SERVICES

University-Level Services

1. Member, Shared Infrastructure Advisory Committee, UF Information Technology, 2011 – 2012.
2. Mentor, University Minority Mentor Program (UMMP), 2008 – 2011.
3. Mentor, SEAGEP Summer Research Experience for Undergraduates (REU), 2008 – 2011.

College-Level Services

1. Steering Committee Member, Interdisciplinary Strategic Planning (Energy), 2009 – 2010

Departmental Services

4. Member, Graduate Admissions Committee, 2005-2011.
5. Member, Scholarships and Awards Committee, 2005-2011.
6. Member, Colloquium Committee, 2005-2011.
7. Commencement Representative, 2004-2006.

SERVICE TO SCHOOLS

1. **Judge**, Alachua Regional Science and Engineering Fair, 2010, 2012.
2. **Judge**, Ft. Clarke Middle School Science Fair, December 07, 2011.
3. **Volunteer**, Talbot Elementary School, Alachua, Florida, 2010-2012.