

# Nanoelectronics Science and Engineering Center

## 1 OVERVIEW

The goals of the proposed center are to create new fundamental knowledge, to invent new concepts, and to design methodologies that can lead to the practical realization of future nanoelectronics based on the deposition of nano-dimension diamond on silicon substrates. The research proposed here has the potential of practical realization of a reversible nanocomputer with three order of magnitude speed improvements over current techniques. The research of the center will revolve around inventing new tools for assembling, processing, modeling and characterizing nanostructures, devices, circuits and architectures. The center will bring together researchers with diverse expertise, in partnership with industry, government laboratories, national and international institutions to address the complex, interdisciplinary challenges in nanoscale materials, devices, circuits and architectures. The center will integrate research with education both internally and through a variety of partnership activities. The center will focus on discovery and technology innovation and will involve a broad spectrum of disciplines including engineering, mathematics, computer science, the physical sciences and biological sciences.

The guiding principle in the selection of researchers is to assemble an interdisciplinary team working in traditional disciplines, and capable of thinking “out-side the box.” The center based at Clemson University and distributed across a number of academic institutions including Georgia Inst. of Tech., North Carolina State Univ., Purdue Univ., Univ. of Florida, Univ. of Texas at Dallas, US Naval Academy, and West Virginia University, will have a well-integrated research and education program. Based on the track records of the participants, NSEC is capable of providing “a whole greater than the sum of its parts.”

Human resource development is one of the missions of the center. The center will incorporate extensive student participation in research. The center will sponsor activities in course and curriculum development and effective partnerships to advance pre-college education, workforce training, and the public understanding of science and engineering, in general and nanotechnology in particular. The center will sponsor activities to foster human resource development and enhance participation of under-represented groups in science and engineering. The desired outcome of the educational program includes new generations of engineers and scientists with the depth and breadth needed for leadership throughout their career in a global economy. To address the problem of demographic changes that are expected to act to the detriment of academic research, we will seek participation of the brightest and the best untenured faculty members. We will invest intellectual and physical resources, so that these individuals can become future academic leaders. Therefore more than one third of the faculty members involved in the NSEC pre-proposal are untenured assistant professors.

### 1.1 Vision

The vision of the center is to create a knowledge base to push semiconductor technology to its limit. The primary emphasis will be to create opportunities in academe to collaborate in a cross-disciplinary, multi-university and industrial setting, and to develop new graduate and undergraduate curricula across traditional disciplines.

### 1.2 Rationale for establishing the Center

As we are about to enter the 21<sup>st</sup> century, complementary metal-oxide-semiconductor (CMOS) based silicon microelectronics has become the driver of economic growth. The importance of microelectronics for future economic prosperity is evident from the fact that each country wants to create its own silicon valley [1]. In principle, silicon MOS transistors with feature sizes as small as 10 nm have been demonstrated [2]. However, there is an open question about how far

the dominance of silicon-based electronics will continue. Any new technology beyond silicon CMOS must provide improved functionality, improved performance, improved reliability and lower cost of future electronic systems.

The answer to the question: “What after Si CMOS?” must be based on fundamental issues as well as “proof of concept” experimental results. In a recent publication [3], Singh and co-workers have examined all the technology options beyond silicon CMOS. As shown by Bates [4], the single particle used for logic or memory applications does not give the lowest error probability for a given total power dissipation. From a heat dissipation point of view, molecular electronics (involving billions and trillions of molecular devices) based on currently explored transistor materials and currently explored computer architectures will burn as soon as it is turned on [5]. The limited experimental demonstration of molecular electronics does not prove that scaling up for practical applications will be easy or possible or that molecular electronics will be competitive with improvements in microelectronics [6]. Although quantum computation has lots of potential, there are still many unresolved fundamental issues [3,7]. Due to the intrinsically error-prone nature of DNA computing, it is highly unlikely to emerge as a practical solution of Si CMOS replacement. Due to a lack of technology to monolithically integrate a diverse set of devices (lasers, lenses, mirrors, crystal etc.) on a common substrate, and the lack of a device equivalent to a static random access memory device, it is highly unlikely that future optical computing can compete with dense silicon integrated circuits [8].

Based on the analysis presented above, the future solution should have the following features: (i) to address the heat dissipation problem, use reversible logic based on diamond (highest known bulk thermal conductivity of any material) transistors; (ii) to address the problem of throughput and defects in nano-lithography, invent a hybrid system [9] based on direct writing [10] and self assembly [11]; (iii) consider fundamental limitations in the design of FETs as well as circuits based on reversible logic; and (iv) use silicon as a substrate to develop nanoelectronics. The research proposed here has the potential of providing the necessary and sufficient fundamental knowledge that can eventually lead to the proof-of-concept breakthrough of new practical devices and systems (parallel to the discovery of transistor in 1948 and the discovery of integrated circuits in 1957). Unfortunately, there is not a single academic research center that deals with all the key issues addressed above. The purpose of our proposed NSEC is to fill the gap of a Center that can provide a team of diverse academic expertise capable of providing a breakthrough in the fundamental knowledge.

### **1.3 Existing and Planned Capabilities of the Center**

In the last 20 years, Clemson University has played a significant part in the human resource development of a large number of graduate and undergraduate students currently employed by the semiconductor industry. The principal finding of the Clemson researchers in the reliability area is that for the fabrication of semiconductor devices with improved performance and built-in reliability, materials with homogeneous microstructures are required [12]. In the semiconductor processing area, we have invented a new thermal processing technique called rapid photothermal processing (RPP)[13]. Part of the RPP technology invented at Clemson University (Dr. Sharangpani, as a Ph.D. student is co-inventor of US patent # 5820942) has been licensed to AG Associates for commercialization. We also have unique expertise in self-assembly, nanoscale characterization of materials, multiscale modeling, electromagnetics and noise interactions, and expertise in surface science. The participating institutions have excellent facilities in Nanoelectronics related areas. The Center of Silicon Nanoelectronics, Electron Microscopy Lab

and the Chemistry department at Clemson University have excellent experimental facilities for conducting nanoelectronics research.

As described in the institution letter of support, Clemson university commitment to the proposed center is at least \$500,000 per year, 6 new faculty positions, 15,000 sq. ft. of laboratory and office space, and additional in-kind commitments, such as faculty time and graduate student support. Thus, with the current and committed resources of Clemson University, equipment purchased from NSF support, as well as the facilities and resources of the participating institutions, NSEC is in a unique position to provide the fundamental breakthrough knowledge in Nanoelectronics.

## **2 PROPOSED RESEARCH OF THE CENTER**

From both speed and heat dissipation point of view, diamond is the best possible semiconductor material [14]. The focus of the proposed research activities of NSEC is to provide breakthrough fundamental knowledge that can lead to a “proof-of-concept” nanoelectronics based on the diamond quantum FET. The research activities will be focused in the following areas: (i) without using any mask, grow defect-free nanoclusters of diamond (with homogenous microstructure) on silicon substrates, as well as develop processes to deposit other related materials (dielectrics and conductors) on diamond nanoclusters that will be used in the fabrication of FET transistors; (ii) provide fundamental knowledge and proof of concept data that the proposed process techniques can be scaled to manufacturable process; (iii) develop critical enabling computational tools that can provide fundamental knowledge to invent new processes; (iv) develop material characterization techniques (with special emphasis on microscopic surface and interface defect detection and control) that are adaptable to a manufacturing environment; (v) investigate phenomena that are barriers in the practical realization of nanoelectronics and provide means to circumvent limitations (if possible) by clever device, circuit, architecture and/or materials designs; (vi) perform first-principles device model calculations taking fundamental limitations into considerations; (vii) learn from biological phenomena that can be of use in the practical realization of diamond-based nanoelectronics; (viii) develop circuit designs and computer architectures and techniques that can eventually lead to diamond quantum FET based reversible logic; and (ix) integrate the knowledge and demonstrate a proof of concept ring oscillator based on diamond nanodimension FETs.

### **2.1 Research Plan**

The proposed research will be focused in the following thrust areas: (i) synthesis and development of new materials, new processes and new equipment; (ii) atomic level characterization; (iii) process modeling; (iv) theory, modeling and conceptual development; and (v) circuit fabrics and architectures.

#### **2.1.1 Synthesis and development of new materials, new processes and new equipment**

Research Team: **Poole** (EE), Singh (EE), Churmanov (Chemistry) Hwu (Chemistry), Luzinov (Textiles), Perahia (Chemistry), Sweryda-Krawiec (Textiles), and Weir (LNL).

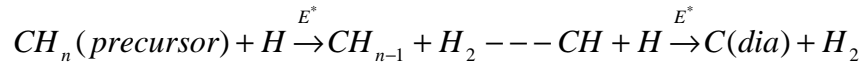
The best strategy to develop future nanoelectronics is to solve the problem of heterogeneous integration of nanodimension diamond with silicon substrates. Unfortunately, so-called crystalline CVD diamond films are actually polycrystalline films with a wide range of crystalline dimensions. Depending on the processing conditions, the polycrystalline films are subdivided as large crystallite films (size of crystallites > 200 nm) and fine crystallites (size of crystallites <20 nm [15]). The grain boundaries in polycrystalline films reduce carrier mobility and make fabrication of efficient devices highly unlikely. Here, we propose to grow diamond nanocrystals by selective seeding, which are free from grain boundaries. In our earlier work [16]

it was shown that diamond can be nucleated selectively at active sites associated with etch pits or deposited nanocrystals. Sun and co-workers have shown that low-energy ion bombardment of the substrate enhances diamond nucleation [17]. In a recent publication [18] it was shown that one can ‘engineer’ ultra-small and crystallographically perfect nanocrystal self-assemblies by careful selection of a film/substrate system under appropriate growth conditions. Thus, using a substrate with an appropriate lattice constant, self-assembled and or directly written nanocrystals of diamond can be grown on silicon substrates. The seeded nanocrystals are expected to be single crystals because of the single nucleation event on a given nanocrystal. The novel idea proposed here is to provide the single nucleation event selectively by controlling the size and chemical characteristics of self assembled and/or directly written nanocrystals.

The concept of pseudomorphic growth [19] will be used to grow device quality defect free diamond nanocrystals on silicon substrates. For materials growth, both self-assembly as well as direct writing approaches will be integrated to grow defect free diamond nanocrystals as well as other materials. In case of self-assembly we will use the inorganic as well as organic approaches [20]. Researchers at Clemson University have extensive experience in the self-assembly of silicon [21], metals [22] and polymers [23]. Recent work shows [24] that cycloaddition reactions widely used in organic chemistry can also be applied to link organic molecules to the (100) surfaces of crystalline silicon, germanium, and diamond.

Direct writing by focused ion beam (FIB) processing has several advantages over other resistless processing techniques. The removal of resist, etch and plasma strip processing steps removes a major obstacle in nanoscale processing. To achieve high throughput, we propose a novel concept based on the use of ultra-fast reaction dynamics (vacuum ultraviolet photo-assisted chemical vapor deposition (CVD)) and multi-source focused ion beam technology for direct writing of different materials. By using VUV assisted CVD we have observed the highest growth rate of Aluminum ever reported (299 nm/sec) with the film resistively comparable to the bulk value [25]. As compared to a standard FIB system, the throughput is increased by more than four orders of magnitude.

Based on our extensive experience in the reduction of defects and increase of bulk and surface diffusion coefficients by the use of vacuum ultraviolet photons in rapid photothermal processing [26], new equipment and processes for self-assembly as well as direct writing will be developed. In the formation of diamond nanocrystals on a silicon substrate, the use of vacuum ultra violet incoherent photons (wavelength in the range of 100-200 nm) will promote the formation of  $sp^3$  bonds as given by:



where  $E^*$  is the energy provided by photons or electrons.

Thus by using VUV photon-dominated self-assembly and direct writing, we expect to achieve defect free growth of nano-crystals of diamond on silicon. In a similar fashion dielectric and metal nanoclusters will be grown to fabricate quantum FETs.

### 2.1.2 Atomic level characterization

Research Team: Narayan (NCSU), Churmanov (Chemistry), Hren (NCSU), Mayo (NCSU), Perahia (Chemistry), Pennycook (Oak Ridge), Shirnov (NCSU).

Atomic arrangements and chemical characteristics of dislocations and grain boundary interfaces play a crucial role in determining the properties of nanocrystalline materials. This information on atomic structure and chemistry is also needed to perform atomic-level engineering of defects and interfaces, and furthermore modify processing parameters to obtain desirable characteristics and properties of materials. Thus, a ‘‘complete’’ nanoscale

characterization of grain boundaries/interfaces, correlations with properties and tuning of the processing parameters to optimize the properties represent unique features of this proposal.

The primary emphasis of our characterization studies will be on determination of atomic structure and chemistry of defects and interfaces. NC State University has a unique facility, the NSF Center for Atomic Resolution Electron Microscopy (directed by J. Narayan), containing a JEOL-JEM 2010 Field Emission Electron Microscope equipped with Gatan Image Filter and x-ray EDS system. In addition, NCSU has two TOPCON 002B electron microscopes – one configured in high-resolution TEM mode (0.18 nm point-to-point and 0.12 nm line-to-line resolution, best available currently at 200 keV) and one in analytical mode for X-ray, EDS, EBIC and cathodoluminescence studies. In the JEOL 2010, we plan to perform STEM-Z contrast and parallel electron energy loss spectroscopy simultaneously for atomic structure and chemistry studies and STEM-Z contrast technique in combination with Parallel Electron Energy Loss Spectroscopy (PEELS). Using a new field emission atomic resolution microscope provides simultaneously atomic structure, chemical information and bonding characteristics down to a resolution of 0.16 nm.

### 2.1.3 Process Modeling

Research Team: **Grujic** (ME), Bachlechner (WVU), Brenner (NCSU), Harrison (USNA), Khan (Mathematical Sciences), Miller (ME), Mintmire (NRL) and Stuart (Chemistry).

The main objective of the proposed computer modeling and simulations activities is to develop a set of novel, fast and reliable computational tools that will enable establishment of the links between process parameters, materials microstructure and properties, and device performance. These tools will initially help explain the findings of the proposed experimental efforts associated with direct writing and self-assembly based processing, the synthesis of the new materials and the effect of processing-induced defects on the performance of devices. The tools will ultimately be brought to the level of physical exactness, sophistication and speed at which they can be used for directing our efforts toward devising new processing schemes, materials microstructures and device architectures. The assembled team has considerable expertise in all of the simulation methods and material systems discussed below. The expertise and experience of Prof. Khan, a mathematician (having contributions in interdisciplinary semiconductor research [27]) will be exploited in inventing new simulation approaches. Initial computer modeling and simulation efforts will address the challenges given below. However, since the field of computer modeling and simulations is very dynamic, it is likely that new additional approaches will also be utilized.

The challenges are: (i) development of multi-length scale modeling and simulation methods capable of covering length dimensions from those of individual atoms and molecules (~0.1nm) to the size of a reactor (0.1 - 1m) and from the temporal dynamics of atomic motion ( $10^{-13}$  s) to that required to build up thin films ( $10^2 - 10^3$  s) [28,29,33]; (ii) development of efficient, parallel, scalable multi-million particle atomistic simulation algorithms with spatial and temporal multi-resolution capabilities to span the required orders of magnitude in length and time [30]; (iii) development of accurate ‘reactive’ interatomic potentials, using both empirical and *ab-initio* approaches, suitable for determination of energy barriers and kinetics of various chemical reactions and embodying the effect of photo-excitation, which promotes formation of  $sp^3$  bonds [31-32]; (iv) development of fast, robust *ab-initio* atomistic simulation methods such as density-functional based molecular dynamics suitable for computation of electronic and thermal materials properties and for validation of critical predictions of the classical atomistic simulation methods [32, 34]; (v) development of combined fluid dynamics/atomic-scale models

for analysis of complex interactions between ions, photons and diamond cluster precursors and collisions of the diamond clusters with the substrate during the focused ion-beam direct writing deposition process [28,29,35]; (vi) atomic-scale simulation of the effect of the grading profile and the layer thickness on atomic-level stresses and formation of crystalline defects such as dislocations and grain boundaries in Si/C graded single crystalline substrates with an increasing carbon concentration on single-crystal silicon substrates [32-34]; (vii) integration of the intramolecular potentials to be developed in part (iii) with optimization methods such as the genetic algorithm to model self-assembly and the resulting self-formation of nano-scale devices [35].

#### **2.1.4 Theory, Modeling, and Conceptual Development**

Research Team: **Frensley** (UT Dallas) Laskar (G.Tech), Hickman (Bio Engineering), Pham (EE), Singh (EE), Wheeler (Biological Sciences).

Within this thrust area we will pursue research that directly supports development of diamond devices, and explores new opportunities in the areas of biological technologies and direct device-device interaction to enable new system architectures. The diamond quantum FET simulations will be provided by W.R. Frensley (University of Texas-Dallas). His team will supply device modeling codes and results of varying degrees of sophistication and interactivity. Fully interactive codes, which implement simple self-consistent energy-band models, will be delivered to the experimentalists, to support device design and experimental data interpretation. More sophisticated device models will be developed and run by the modeling group for the purpose of quantitatively assessing the performance capabilities of the diamond quantum FET. These models will include the details of the band structure, size unitization effects, and self-consistency of the potential. Because transistors are necessarily open quantum systems (electrons must be free to flow into and out of them), techniques for treating open quantum systems will be employed [36].

To address the problems of signal communication and clock distribution in nanosystems, another part of this thrust will investigate direct device-to-device interactions, under the direction of Prof. J. Laskar (Georgia Tech) and Prof. A.V. Pham (Clemson). The research tasks will include: (i) develop circuit models to study coupling phenomena; and (ii) invent device-to-device communication mechanisms, including micro-machined wave-guide structures operating into THz frequencies and beyond. For chip-to-chip communications, the research will focus on defining the "system level" interface: transmit/receive requirements, power dissipation, interface management and design rules for integration into diamond-based circuits.

Profs. J.J. Hickman and A.P. Wheeler (Clemson) will explore biological phenomena that may be useful in the development of diamond-based nanoelectronics. Examples are programmed cell death or apoptosis [37] and an understanding of the mechanisms that make protein function so robust against thermal motion [38] will be targeted. The understanding of programmed cell death may lead to a new self-assembly technique where the cell death in the selected region of a film may provide a patterned surface. The second topic may provide concepts that can lead to processes and devices that can be robust against thermal fluctuations.

#### **2.1.5 Circuit Fabrics and Architectures**

Research Team: **Roy** (Purdue), Frank (UF), Smotherman (CS).

The challenges presented by nanoscale diamond FET devices to circuit designers and to computer architects are numerous. With the diamond FET devices described, we must address issues that start at the point where the International Technology Roadmap for Semiconductors (ITRS) ends. Our major thrust will be in applying reversible computing to the circuit design and architecture of nanoscale computers. Reversible techniques offer scalable energy efficiency and,

when applied at all levels, offer arbitrarily high factors of reduction in the power required per unit of throughput [39-43]. For example, if we consider a power dissipation constraint of 1 W/cm<sup>2</sup> (so that a reversible computer with a 10-cm<sup>2</sup> footprint would only use 100 W, comparable to today's desktops), then a 10 cm-thick stack of nanoelectronic circuits could ideally be ~5,000 times faster if operated fully reversibly. Impressive gains even with partial reversibility can be found by careful selection of appropriate circuits on which these techniques can be applied.

For the diamond FET, circuit techniques applicable at the nanoscale level include gated-V<sub>dd</sub> and dynamic scaling of supply voltage. Gated-V<sub>dd</sub> techniques use an extra transistor between the logic and supply or ground terminal. The transistor is turned on during regular operations and it is turned off during idle mode to virtually eliminate leakage in low threshold designs. The power supply voltage and clock frequency of each computational element (CE) can also be scaled based on directives from hardware monitors to meet the power performance requirement at any given time. Moreover, a dynamic selection can be made among different CEs or software routines exercising the CEs. Our preliminary results on a dynamically reconfigurable (DRI) cache using gated-V<sub>dd</sub> technique shows that 100 X improvement in leakage can be obtained without sacrificing performance [44].

## **2.2 System Level Focus for the Center**

The fundamental knowledge generated by various thrust areas will be integrated to fabricate sub-50 nm feature size diamond based transistors. In addition to our own work, we will collaborate with various industries (for example Texas Instruments, KLA-Tancor etc.) for the fabrication and testing of ultra small dimension devices. The main focus of research at the system level will be related to the fundamental understanding of process integration. The end product of the research component of the Center will be the fabrication of a sub-50 nm feature size ring-oscillator that is based on the science and technology developed by NSEC.

## **3 PROPOSED EDUCATION ACTIVITIES OF THE CENTER**

In order to address the issues of paradigm shifts in higher education (for example e-learning), we propose the following. First, we will consciously put into practice the lessons of various initiatives, sponsored by NSF and other agencies and organizations, which have shown that the “interactive-engagement” approach is much more effective in education than the lecture setting. We will build upon our already successful programs, Program for Educational Enrichment and Retention (PEER) and Women in Science and Engineering (WISE) to encourage minority students and women to fully participate in the NSEC program.

### **3.1 Undergraduate Education**

Currently we offer a number of courses that relate directly to nanoelectronics. We propose to develop several lower-level interdisciplinary introductory courses based on an “interactive-engagement” approach. One example is a course entitled “Nanotechnology-Driven IC Fabrication”, which would have the following features: (i) interdisciplinary team teaching; (ii) hands-on laboratory experience to acquaint the students with real manufacturing issues; (iii) an emphasis on collaborative learning and working; (iv) an emphasis on showing how manufacturing techniques continually evolve with a better understanding of what actually occurs in the processing; and (v) an emphasis on the importance of reflection and integration of experience to achieve understanding. The objective of such courses will not be to deliver a “complete set of state-of-the-art facts”, but rather to stimulate the students to observe, ask questions, and then actively seek answers.

### **3.2 Graduate Education**

In order to attract graduate students, a number of NSEC/NSF fellowships will be awarded to

participating NSEC institutions. In addition to upgrading our current courses in microelectronics, new interdisciplinary courses will be introduced. A distinct feature of the on site training and courses will be embedded in the concept of “delivery of information just in time.” Courses will not be restricted to the traditional semester, but offered as and when necessary to suit an industrial client. The Center will bring several industrial experts on campus for short periods of time (less than one week at a time) to interact with students and faculty. After the Center is established, NSEC will work in conjunction with our continuing education program to provide lecture-type courses (both on-campus and off-campus) and hands-on short-term courses.

### **3.3 K-12 Education**

In the area of K-12 education we will work with our existing programs within the state of South Carolina and start new programs. The following Programs will be implemented: (i) the South Carolina State Systematic Initiative; (ii) South Carolina Center of Excellence; and (iii) Southeastern Consortium for Minorities in Engineering, Inc. A special committee chaired by Dr. Harold Cheatham, Dean of the College of Health, Education, and Human Development or his representative will guide our K-12 program.

### **3.4 Integration of Research and Education**

The objective of this program is to create an integrated multidisciplinary educational program in nanoelectronics. The program emphasis will be on: (i) fundamental engineering physics and chemistry that are important at nanodimensions; (ii) new ways of creating products by nanomaterial synthesis capabilities; (iii) new range and functionalities of products that can potentially be created by nanomaterials; and (iv) introducing an “out-side -the box” approach to thinking. The interdisciplinary faculty will provide a comprehensive education and research training program including six new specialized courses and integrated research experiences. These classes will involve a diverse set of topics such as “nano-material processing.” These students will participate in the formal classroom and laboratory training, an industrial and federal-laboratory internship, a bi-weekly interdisciplinary seminar, and international educational experiences. The undergraduates will participate in ongoing projects as well as pursue independent projects.

### **3.5 Development of Human Resources**

Human resource development (K-12 students and their teachers, undergraduate and graduate students, post doctoral fellows as well as mentoring of junior faculty members) is one of the prime missions of the NSEC. In conjunction with ongoing national as well as local programs, special attention will be paid to providing recruitment, retention, and leadership opportunities to under-represented -groups. We will capitalize our strength in integrating communication skills in all of our classes. Clemson University integrates writing, oral, visual and electronic communication in all disciplines and was named recently as the “Public College of the Year” by the Time Magazine. In collaboration with Clemson's Spiro Center for Entrepreneurial Leadership, our College of Business and Public Affairs faculty will revise Entrepreneurship courses to meet the needs of NSEC students. By working with industry experts and patent attorneys we will teach “intellectual property and copyright” related concepts to NSEC students.

## **4. TECHNOLOGY TRANSFER, INTERNATIONAL COOPERATION AND CENTER MANAGEMENT**

### **4.1 Technology Transfer**

In addition to the exchange of personnel between NSEC and industry, we will start a new certification program (through our continuing engineering education) whereby industrial workers

can obtain practical training in the area of nanoelectronics. This innovative program will involve practical hands-on experience as well as lectures in the classroom. A professional apprenticeship program will be initiated to provide students with the opportunity to accept industrial work assignments. The intent of this program is for students to learn how to work in the industrial environment and thereby broaden their educational experience. Faculty members will be encouraged to spend time at industrial sites because students benefit tremendously from instruction by teachers with both academic and industrial experience. The publication and distribution of a periodic newsletters, the organization of conferences and workshops (NSEC alone or in collaboration with other organization), an annual review meeting, visiting NSEC labs, and telecampus courses (via two-way video communication) available for industrial workers as well as for the academic community) are additional tools that will be used for tech-transfer.

#### **4.2 Cooperation With International Institutions**

We will keep close contact with the government-funded International Technology Research Institute of Loyola College of Maryland for keeping track of strategic cooperation partners. Initially, we have made contacts to cooperate with the Center for Excellence in Nano/Microelectronics and Laboratory of Semiconductor components (Dr. Sorin Cristoloveanu and Dr. Francuis Balestra, UMR CNRS/INPG, Grenoble, France), IMEC (Prof. C. Claeys, Belgium), the Energenius Center for Advanced Technology (Prof. Harry Ruda, University of Toronto, Canada), Delft Institute of Microelectronics and Submicrontechnology (Prof. C.I.M. Beenakker, Delft University of Technology, Netherlands), Center for the Nanoscale Science and Technology (Prof. Ken Snowdown, Univ. of NewCastle upon Tyne, Australia ), Institut fuer Neue Materialien gem. Gmbh (Prof.Helmut Schmidt, Germany), Prof Hiroshi Iwaih of Tokyo Institute of Technology, Japan, Prof. Ayako Kimura of Keio University, Japan, Prof. C. Jagdish of Australian National University, Prof. Samres Kar of I.I.T. Kanpur, India and Prof. Ninoslav Stojadinovic of University of Nis, Yugoslavia.

#### **4.3 Center Management**

The Center Director, Dr. Rajendra Singh, will provide primary administration and management of the Center. The management team consist of an Industry Liaison Coordinator, Dr. Kelvin F. Poole (Dr. Poole has extensive administration expertise and industrial contacts, including ex-chair of the Department of Electrical and Computer Engineering), an Education Coordinator, Dr. Joseph R. Manson, (winner of 1998 South Carolina Governor's award for Excellence in Science discovery) and Thrust Leaders. The Technical Advisory Board members consist of Dr. Robert Doering (Chair), Texas Instruments, Dr. Lin Swanson, FEI Co, Dr.John Fan, Kopin Cooperation, Dr. Stephen Pennycook, Electron Microscopy Group Leader, Oak Ridge National Laboratory; and Dr. Kamal Rajkanan, Managing Director, KLA-Tencor. As former Director of the Materials Science and Engineering Program, the NSEC Director, Dr. Singh has extensive experience in nurturing interdisciplinary activities at Clemson University.

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## **BRIEF BIOGRAPHICAL SKETCH OF THE CENTER DIRECTOR**

Dr. Rajendra Singh is D. Houser Banks Professor of Electrical and Computer Engineering and Director of the Center for Silicon Nanoelectronics. Prof. Singh has over 20 years of industrial and academic experience in semiconductor technology. He is author of over 250 publications. Dr. Singh is chair of IEEE EDS Semiconductor Manufacturing Technical Committee and member of IEEE EDS Nanotechnology Technical Committee. In 1998 he received Thomas D. Callinan Award of the Electrochemical Society. He is a Fellow of the Society of Optical Science and Engineering, American Association for the Advancement of Science, and ASM International, the Materials Information Society.

## **LIST OF PARTICIPATING INVESTIGATORS**

### ***(A) CLEMSON UNIVERSITY***

Dr. Rajendra Singh	D. Hoser Banks Professor, Electrical and Computer Engineering
Dr. Kelvin F. Poole	Professor, Electrical and Computer Engineering
Dr. Anh-Vu Pham	Assistant Professor, Electrical and Computer Engineering
Dr. Mica Grujicic	Professor, Mechanical Engineering
Dr. Richard S. Miller	Assistant Professor, Mechanical Engineering
Dr. James J. Hickman	Hunter Chair Associate Professor, Bioengineering
Dr. Joseph R. Manson	Professor, Physics
Dr. Allfred P. Wheeler	Professor, Biological Sciences
Dr. Shou-jyh Hwu	Associate Professor, Chemistry
Dr. Steven J. Stuart	Assistant Professor, Chemistry
Dr. Dvora Perahia	Assistant Professor, Chemistry
Dr. George Chumanov	Assistant Professor, Chemistry
Dr. Mark K. Smotherman	Associate Professor, Computer Science
Dr. Taufiqar Khan	Assistant Professor, Mathematical Sciences
Dr. Igor Luzinov	Assistant Professor, Textiles Fiber and Polymer Science
Dr. Beata Sweryda-Krawiec	Research Associate/Assistant Professor
Dr. Nagraj. Balakrishnan	Professor, Management
Dr. Caron H. St. John	Professor, Management

### ***(B) NORTH CAROLINA STATE UNIVERSITY***

Dr. Jagdish Narayan	Distinguished Professor, Materials Science and Engineering
Dr. John J. Hren	Professor, Materials Science and Engineering
Dr. Donald W. Breener	Associate Professor, Materials Science and Engineering
Dr. R. Mayo	Associate Professor, Materials Science and Engineering
Dr. V. Shirmov	Research assistant Professor

### ***(C) PURDUE UNIVERSITY***

Dr. Kasha Roy	Associate Professor, Electrical Engineering
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### ***(D) UNIVERSITY OF FLORIDA***

Dr. Michael P. Frank	Assistant Professor, Computer and Information Sc. and Eng.
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**(E) UNIVERSITY OF TEXAS - DALLAS**

Dr. William.R. Frensley      Professor, Electrical Engineering

**(F) GEORGIA INSTITUTE OF TECHNOLOGY**

Dr. Joy Laskar      Associate Professor, Electrical and Computer Engineering

**(G) WEST VIRGINIA UNIVERSITY**

Martina E. Bachlechner\*      Assistant Professor, Physics

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**(H) US NAVAL ACADEMY**

Dr. Judith Harrison      Associate Professor, Chemistry

**(I) NAVAL RESEARCH LABORATORY**

Dr. John Mintmire      Research Physicist

**(J) OAK RIDGE NATIONAL LABORATORY**

Dr. Stephen J. Pennycook      Electron Microscopy Group Leader

**(K) LAWRENCE RIVER NATIONAL LABORATORY**

Dr. Samuel T. Weir      Staff Physicist

## **SYNOPSIS OF INSTITUTIONAL COMMITMENTS**

Clemson University is pleased to give its full endorsement of and support for the Nanoelectronics Science and Engineering Center (NSEC). The university commitment to the proposed center is at least \$500,000 per year, six (6) new faculty hires in areas of expertise critical to the proposed research programs, 15,000 sq. ft. of laboratory and office space, and additional in-kind commitments, such as faculty time and graduate student support. Additional support from the State will be sought through the legislative process.

The proposed center will provide an integrated environment for the systems-oriented study of materials, processes and products related to nanoelectronics. The research and education strategies are designed to make fundamental advances that will lead to further innovation in industry. NSEC will create an enriched environment that integrates the ideas of university faculty, industry researchers, graduate and undergraduate students. Center research and education cut across engineering and science cultures and disciplines to produce a new generation of engineers and scientists better prepared to meet the challenges of the nanoelectronics industry in the 21st Century. The proposed center's research results and the associated graduates will be strategically aligned with the economic development plans of the State of South Carolina.

The College of Engineering and Science was formed in 1995 by combining the existing engineering departments with the physical and mathematical/computational science departments, as well as the School of Textiles. This new administrative unit has significantly enhanced cross-disciplinary research and educational activities. Many of the traditional administrative and cultural barriers between engineering and science have been eliminated. The effectiveness of the new college has been demonstrated over the last three years by the success of the National Science Foundation/Engineering Research Center (NSF/ERC) for Advanced Engineering Fibers and Films. The lessons learned in the start-up and operation of this center will be applied to the proposed Nanoelectronics Science and Engineering Center.

## **BUDGET EXPLANATION**

For the first five years we have requested \$20 million from NSF. Georgia Institute of Technology, North Carolina State University, Purdue University, the University of Florida, the University of Texas at Dallas, the US Naval Academy, and West Virginia University are our partner institutions. The five years total budgets of Georgia Institute of Technology, North Carolina State University, Purdue University, the University of Florida, the University of Texas at Dallas, the US Naval Academy, and West Virginia University are \$0.75 million, \$1.697235 million, \$1.25 million, \$0.75 million, \$0.75 million, \$0.325 million, and \$0.325 million respectively. The total amount of sub-contractors is about 30% of the \$20 million requested from NSF.

Human resource development is a very critical area. Therefore, the major part of the requested funds (~46%) will be used in educating and training postdoctoral fellows, graduate and undergraduate students, and K-12 teachers. Overall each year, 8 postdoctoral fellows, 50 graduate students and 50 undergraduate students will be supported by NSF funds. In order to increase the participation of brightest and the best US citizens and permanent residents in to NSEC graduate program, we will offer 10 Fellowship (\$5,000 each) to supplement National or local Fellowships. A typical example of national fellowship is the National Defense Science and Engineering Fellowship program in Nanotechnology. Potential graduate students from all participating NSEC academic institutions can compete for these Fellowships. In order to increase the number of underrepresented groups, we will work closely with a number of ongoing national and local programs. We plan to invest about 8% on our undergraduates. In addition to hiring undergraduates during the academic year, we will also recruit 20 undergraduate students for the summer program. Clemson University and participating academic institutions have several summer research programs funded by NSF. In areas that directly relates to NSEC research activities, we will provide supplemental resources for undergraduates. These students will be selected on a national level competition. Approximately 26% of the budget requested from the NSF will be used in support of faculty salary and staff members. About 18% of the budget will be used in materials, supplies, travel, and communication etc. The existing laboratory facilities and infrastructures are excellent to start the proposed research and the \$2.1 million in equipment money will be used in developing and acquiring new equipment. Apart from the annual meetings with participants to disseminate knowledge, 0.1% of the budget will support an international conference at which worldwide participants will bring the latest developments to the attention of all researchers.

In the first five years, Clemson University will recruit six new faculty members in areas related to NSEC research and educational activities. Three of the faculty members will be recruited in the semiconductor processing areas, one in the area of circuit design, one in the area of computer architecture and one related to the high resolution transmission electron microscopy of nanomaterials.

The Director will manage the Center with the help of a small staff responsible for the following: (i) the maintenance of the NSEC facilities; (ii) budgets; (iii) industry collaboration and technology transfer; and (iv) the educational and human resource development mission of the NSEC. The four staff members i.e., the Technical Manager (responsible for the maintenance of the NSEC research facilities and providing technical links with industrial equipment vendors),

the Accountant (responsible for the budget related financial responsibilities), the Industry Liaison Assistant (responsible for the technology transfer, industrial relations and incubator research related responsibilities), and the Administrative Assistant (responsible for all other day to day activities) will assist the Director in carrying out the mission of the Center. Thus to support NSEC, Clemson University will recruit four staff members, i.e. the Technical Manager, the Accountant, the Industry Liaison Assistant, and the Administrative Assistant. In matters related to intellectual property, and copyrights etc, the Industry Liaison Assistant will also work closely with the Office of Technology Transfer at Clemson University. Other than the Industry Liaison Assistant, the other staff members will be supported by NSF funds.

The equipment money requested from NSF will be used to develop new processing and characterization equipment. As an example, based on the fundamental research done at Clemson University, Xerox Corporation and Matteson will develop a new chemical vapor deposition system (CVD) system capable of providing defect-free, uniform, and low stress, pseudomorphic growth of  $\text{Si}_x\text{C}_{1-x}$  on silicon substrates. Xenon Corporation will provide vacuum ultra violet energy sources meeting the specification of our CVD system. As a leader in CVD and rapid thermal processing, Matteson will integrate the CVD system based on our specifications. Clemson University has extensive experience in the design and assembly of CVD systems. The new CVD equipment will have in-situ RHEED and in-situ AFM capability. Since the CVD system will be based on rapid photothermal processing, the substrate temperature will be used as a chemical switch to control the properties of deposited material. Thus, optimized heating and cooling rates will be used in the growth of different materials. With both in-situ as well as ex-situ characterization, the new equipment will provide a surface that will have flatness at the atomic level.

In another example of equipment development, FEI will build a new generation of direct writing focused ion beam system. The design of the equipment will be based on the findings of Clemson researchers. This new equipment will be capable of demonstrating that as compared to conventional direct writing equipment, the new equipment is capable of providing defect free high throughput nanomaterials. The new system developed for the growth of materials by self-assembly approach will be capable of transferring the sample in-situ from one equipment to another. Thus, the CVD system, direct writing system, and self-assembly system will have the capability of integration by cluster tool concept. Various equipments that will be developed at NSEC is based on the cluster tool concept. This integration approach will allow us to investigate the equipment manufactured by any vendor. As an example, we plan to investigate the Oxford Applied Research's nanocluster source, the NC 200. This equipment has the capability of providing metal cluster in the dimension of 3-4 nm. In another investigation, the NSEC cluster tool will be capable of investigating the role of gas cluster ion beam (manufacture Epion Corporation) on the nucleation of nano-dimension diamonds. Overall with the equipment requested in this proposal, our in-house facilities and the facilities of our collaborators, we will have all the necessary equipment to successfully complete the mission of the Center.