IMAPS Int'l Advanced Technology Wkshp. on Flip Chip Technology
March 12-14, '99 Brasselton GA

# Transmission Line Clock Driver

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**February 24, 1999**

**Abstract**

Clock distribution is a major issues in digital systems. Designers must distribute a square-wave with low skew and fast transition times across very wide chips. And they want to do so, wasting as little power as possible. In most systems, engineers trade power for clean transitions. For example, a common micro-processor chip, like the Alpha, expends 40% of its power on distributing a square-wave across a 1.5cm die.

In this paper, I will describe a new clock distribution technique utilizing resonant transmission lines and flip-chip style connections. This technique reduces clock skew and allows faster transitions over larger chip surfaces. Most importantly it reduces power consumption by up to an order of magnitude over standard drivers.

The paper begins with the motivation for tackling power consumption in clock drivers. I follow this with a description of the current method of driving a clock load. Then I focus on how the transmission line clock driver works. Finally, I wrap up with a brief description of future work.

## 1. Motivation for Resonant Transmission Line Clock Drivers

A number of trends has increased the amount of power consumption of clock drivers. First, clock capacitance has steadily increased as die size and gate capacitance have become larger. Second, the clock frequency is increasing. Clock drivers on current micro-processor chips must drive a 4nF load at 500MHz. This burns almost 20W or 40% of the overall chip power.[i]

Researchers have explored many ways of reducing power consumption. Arguably the simplest way has involved reducing the power supply voltage. This provides a square reduction in power, but adversely affects circuit speeds and increases sub-threshold leakage. Other methods temporarily stop driving unused sections of the chip. Unfortunately, this complicates design and increases the amount of clock skew between chip sections.

On a different topic, a relatively new approach to coordinate different chips at a system level involves using a resonant cavity. Vernon Chi at the University of North Carolina resonates a uniform transmission line with a single sinusoid.[ii] Because the entire transmission line crosses zero simultaneously, this structure can synchronize individual chips throughout the system. Unfortunately, a sinusoidal waveform cannot be used to drive individual clock loads directly, because its transition times are just too long.

In this work I take the resonant approach the next step. Namely, I use a resonating transmission line to drive the large clock capacitance directly. This requires resonating a square-wave instead of a single sinusoid.

There are two major benefits. First, the half crossing occurs simultaneously across the central section of the transmission line. With the help of flip-chip connections this translates to virtually no skew across a single die. Second, the power to drive the on-chip capacitance, comes from the transmission line instead of the power supplies. Therefore, the power consumption falls to just the amount burnt in the parasitic resistance of the transmission line.

## 2. Standard Clock Driver

A standard clock distribution structure appears in Figure 1. It includes a clock generator, a buffer chain, a distribution network and a capacitive load. I have drawn the clock lines in the distribution network as transmission lines even though the series resistance dominates over the inductance.

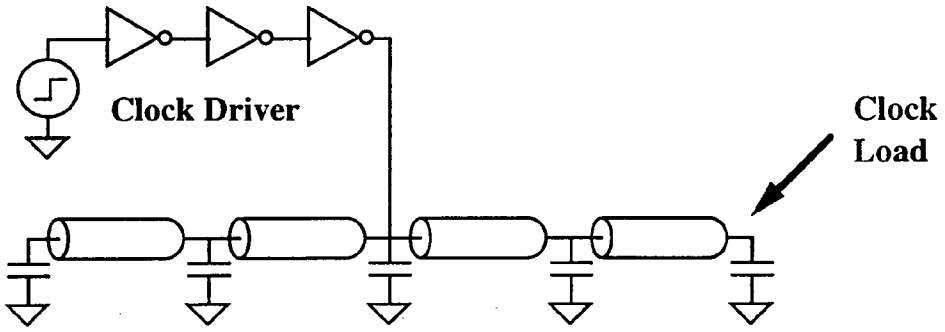


**Figure 1. Standard Clock System for Large Chips**

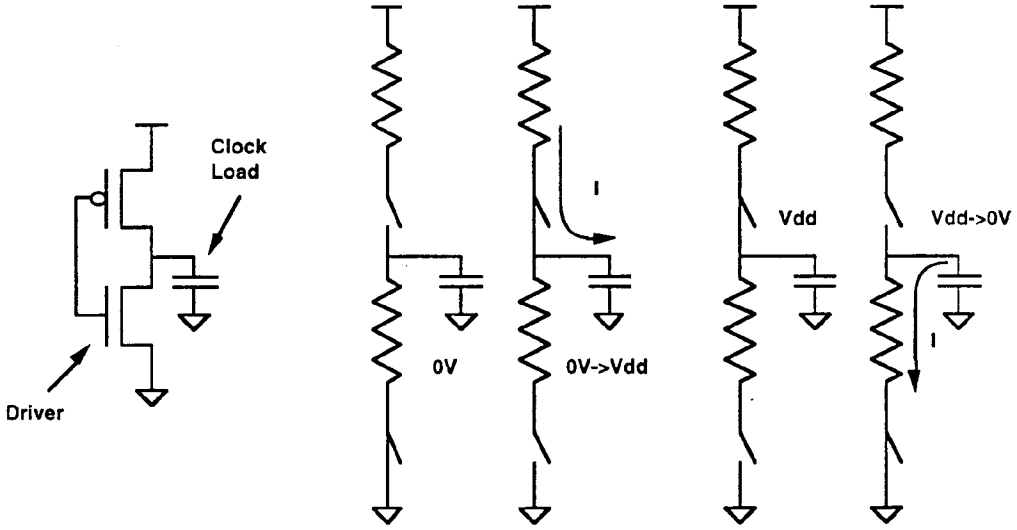


**Figure 2. Power Consumption in Standard Clock System**

Figure 2 shows the crux of the power problem. I have modeled each inverter transistor as a resistor in series with a switch. Current to fill up the clock capacitance comes from the power supply through the p-device resistance, where $1/2CV^2$ is

burnt. This same amount of power is burnt when discharging the capacitance through the n-device resistance. Almost 40% of the chip power gets burnt in this way.

## 3. Transmission Line Clock Driver

Our technique shown in Figure 3, simply adds an external transmission line to the standard clock structure. We recover power by charging and discharging the final clock load not through the clock driver but with the transmission line as seen in Figure 4. This also means that the clock buffers can be smaller resulting in less pre-driver power.

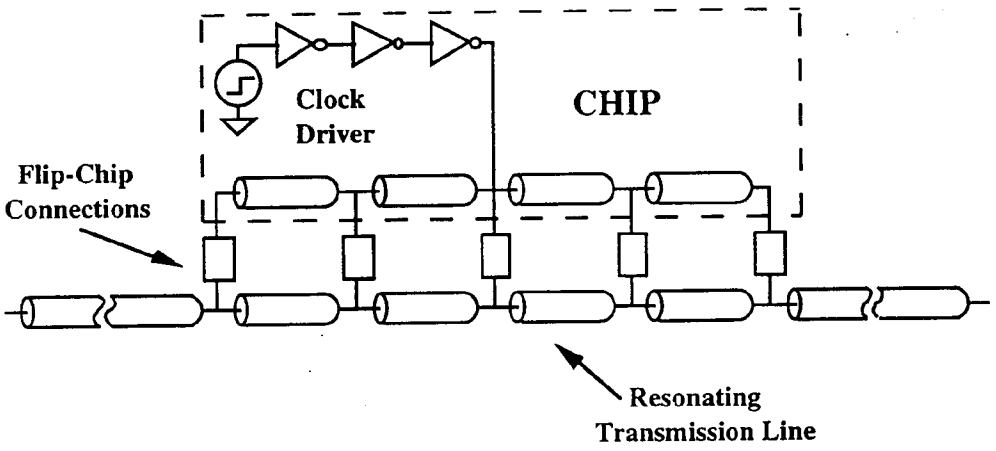


**Figure 3. New Transmission Line Clock System**

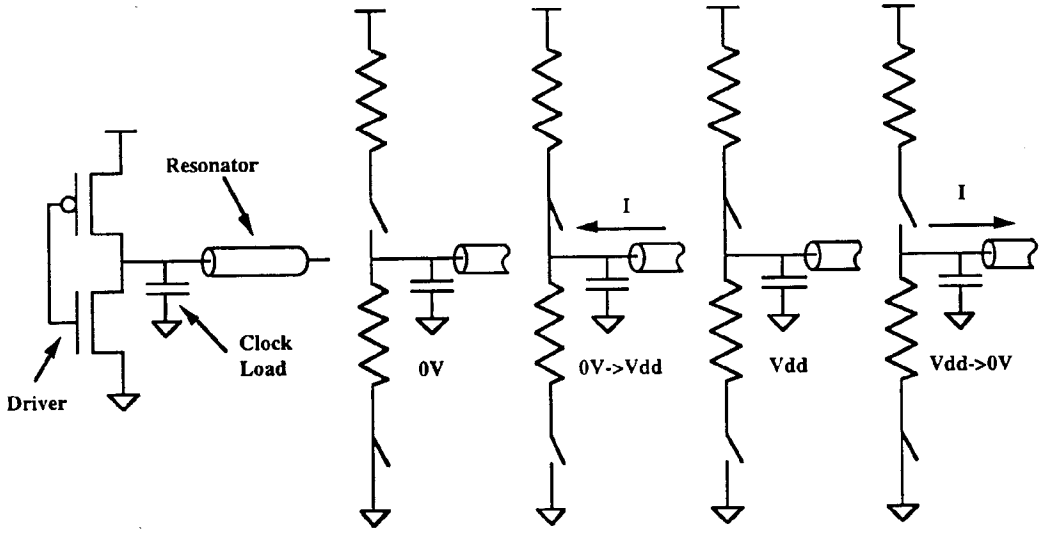


**Figure 4. Power Consumption with Transmission Line Technique**

Let me walk through a brief description of how the technique works. The central driver forces a square wave into the chip and the external transmission line.

Because the driver is small, it cannot initially drive the system to vdd. However, a reduced height pulse flows down the length of the transmission line. The pulse travels to the open termination at the end of the transmission line and reflects back towards the chip. The line length is such that the pulse in the transmission line will reach the driver exactly when it drives again. The result is an increase in the pulse height. Eventually the transmission line will be resonating a full clock pulse at a given clock frequency.

Flip-chip connections strap the internal clock line to the external transmission line. Because modern digital systems need square-wave frequencies over 100 Mhz with fast rise times, a low inductance connection into the chip is critical. Further, flip-chip bumps can be spread across the entire die which significantly reduces skew.

### 3.1 Tuning

Unfortunately, the simple setup presented in the previous section works only in the ideal case. An actual transmission line has parasitic resistance that varies with frequency. Namely, lower frequency signals encounter less parasitic resistance and, in turn, travel more quickly along the line. Since a square wave is the sum of odd harmonics, its frequency components will take different amounts of time to travel the length of the line. Hence, they will arrive back at the source slightly out of phase and fail to produce a clean square wave.

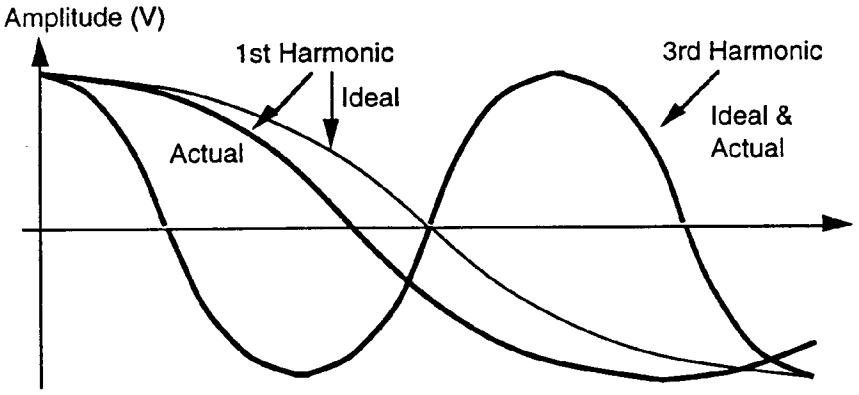


**Figure 5. Voltage in a Uniform Line Tuned for 3rd Harmonic**

Figure 5 shows the effect of parasitics in a line tuned for the third harmonic. In the ideal case, without parasitic resistance, the line will resonate both the 1st and 3rd harmonics. A standing waveform will appear in which the 1st harmonic reaches $\pi/2$ exactly when the third harmonic reaches $3\pi/2$. With parasitics, the line must be longer to resonate the third harmonic at $3\pi/2$. By that point, the faster 1st harmonic will have passed $\pi/2$. In Figure 5 the x-axis represents phase not distance.

One way to realign the waveforms is to introduce a phase shift into just the 1st harmonic. I have discovered a simple method for doing just that. It involves

varying the impedance along the length of the transmission line as shown in Figure 6.

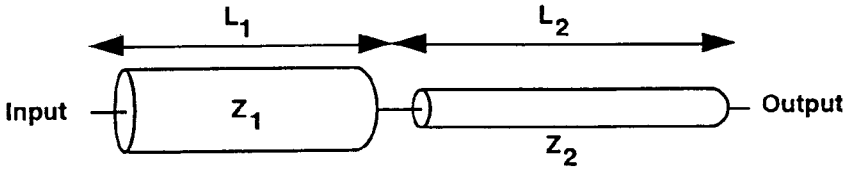


**Figure 6. Transmission Line with Impedance Variation**

Three facts are applicable to describing the voltage and current in the line and more particularly at the discontinuity. First, the voltage and current are continuous. Second, the standing waves are sinusoidal as a function of distance. Third, the voltage and current are related by a derivative and Z. At the discontinuity, this leads to the equation for voltage:

$$V_1 \cos\left(\frac{2\pi f}{vel}x\right) = V_2 \cos\left(\frac{2\pi f}{vel}x + \Delta\Phi\right)$$

and current:

$$\frac{V_1}{Z_1}\sin\left(\frac{2\pi f}{vel}x\right) = \frac{V_2}{Z_2}\sin\left(\frac{2\pi f}{vel}x + \Delta\Phi\right)$$

The 1st equation establishes the voltage continuity across the variation. The second equation basically describes the slope of that voltage across the discontinuity and how it changes by the ratio of the impedances. So, if going into the variation I had a voltage slope of 3 and $Z_2/Z_1$ is 2, then the slope in the next section would be 6. To support this relationship requires a different phase and voltage amplitude across the discontinuity, hence the use of $V_2$ and $\Delta\phi$.

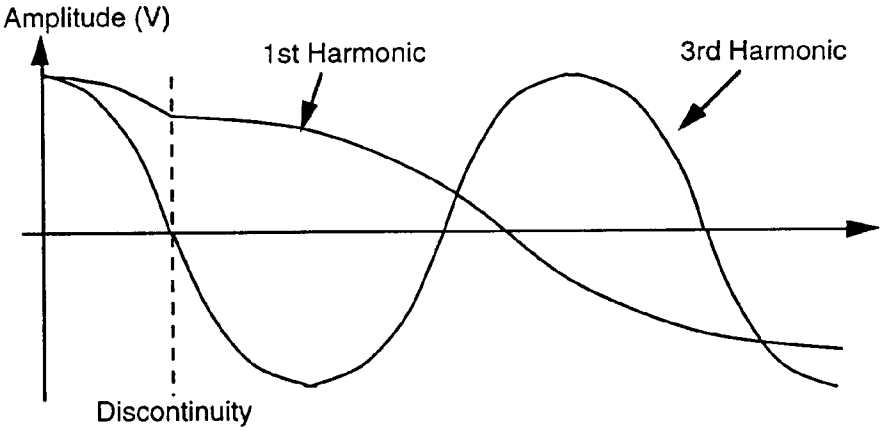


**Figure 7. Impedance Discontinuity for Tuning Line**

Figure 7 shows how this tuning technique would apply to the 1st and 3rd harmonics of our square in a line with parasitics. Since the discontinuity is located

at the 3rd harmonics zero-crossing, its phase cannot be affected. Zero always equals zero. However, the **1st** harmonic experiences a phase shift so that it reaches $\pi/2$ exactly when the third harmonic reaches $3\pi/2$. In this case the impedance ratio would need to be smaller than one.

In order to create a clean square wave, more than two frequencies are required. Because each frequency has a different value for phase and voltage, a discontinuity will affect each by varying amounts. So, the interaction between a number of variations can be used to tune for many more frequencies.

## 4. Future Work

Last year we built a large scale mockup to assess the viability of this technique. It proved very successful in that we were able to reduce power consumption by a factor of 9.5 over a standard driver. The test consisted of an off-the-shelf inverter part driving a string of discrete capacitors. The transmission line was built from many 75Ω twisted pairs ganged together. Because our operating frequency was only 20MHz the entire line stretched across the entire room.

This summer we hope to test a more realistic mockup running at 1GHz. Just last month we submitted a test chip to Mosis in HP's 0.35µm process. The chip contains a slice of a standard clock driver loaded by a large number of flip-flops. We have placed arbiters at the center and edge of the chip to measure clock skew. The power can be measured by observing the current entering the power supplies.

The chip will be bonded using flip-chip bumps to a ceramic substrate that contains our transmission line and i/o. Variations in the width of the line will provide our tuning discontinuities.

## 5. Conclusions

Clock distribution represents an important aspect of digital system design. Current techniques have stalled in their effort to reduce clock skew, transition times and power consumption. A new clock distribution technique utilizing resonant transmission lines can further these goals. It can match the waveform quality of a standard clock driver for a tenth of the driver width and a tenth of the power. Furthermore, skew can be virtually eliminated.

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[i] Bowhill and Gronowski. *Practical Implementation Methods and Circuit Examples used on the ALPHA 21164.* VLSI Circuits Workshop. Digital Semiconductor

[ii] Chi, Vernon. *Salphasic Distribution of Timing Signals for the Synchronization of Physically Separated Entities.* US Patent #5,387,885. University of North Carolina. Chapel Hill, NC 1993.