# SYLLABUS: CDA 5155, Computer Architecture Principles
## Spring 2013

**Description:** This course teaches students fundamental knowledge in computer architecture and microarchitecture. The course covers the basic organizations of computer systems including instruction-set architecture, execution pipeline, memory hierarchy, and I/O subsystem. It also addresses advanced processor microarchitecture issues such as dynamic instruction scheduling, branch prediction, lock-up free caches, instruction-level parallelism, multiple instruction fetch/issuing, speculative execution, etc. to improve computer processor performance. Shared-memory multiprocessor systems with coherent caches to reduce memory access latency are also covered. Finally, it outlines the verification issues of today's microprocessors.

**Prerequisites:** CDA 3101 (Computer Organization), COP 3530 (Data Structures and Algorithms), and strong programming knowledge is required. Knowledge of "compilers" and "operating systems" (COP 4600) is helpful but not required.

**Instructor:** Dr. Prabhat Mishra CSE E568 (352) 505 1880 prabhat@cise.ufl.edu

**Course Office Hours:** Wednesday 1:55 – 3:50 PM or by appointment.

**On-Campus Class Meeting Times and Location:** Tuesday at Period 7 (1:55-2:45) and Thursday at Period 7-8 (1:55-3:50) in CSE 118.

**Course Web Site:** http://www.cise.ufl.edu/class/cda5155sp13/index.html

**Textbook:** Computer Architecture: A Quantitative Approach, **5**th edition, John Hennessy, David Patterson, Morgan Kaufmann Publishers, ISBN: 9780123838728. The fifth edition is required.

**Outline of Course Topics:** The following topics will be covered (in that order). Specific reading materials are outlined for each topic. The links to the lecture slides will be available from the course webpage in just-in-time fashion during the semester.

1. Fundamentals of Computer Design
   - Chapter 1 of the textbook.
2. Instruction Set Principles
   - Appendix A of the textbook.
3. Pipelining: Basic and Intermediate Concepts
   - Appendix C of the textbook.
4. Instruction-Level Parallelism and Its Exploitation
   - Chapter 3 of the textbook.
5. Review of Memory Hierarchy
   - Appendix B of the textbook.
6. Memory Hierarchy Design
   - Chapter 2 of the textbook.
7. Multiprocessors and Thread-Level Parallelism
   - Chapter 5 of the textbook.

8. Data-Level Parallelism: GPU Architectures
    - Chapter 4 of the textbook.
9. Storage Systems
    - Appendix D of the textbook.
10. Verification of Processor/Memory Architectures
    - Reading material will be provided.

**Grading Criteria:** The final grade will be on the curve. Both regular grades (e.g., A, B+, B etc.) as well as minus grades (e.g., A-, B- etc.) will be used. Typically top 20% students will receive A, next 15-20% students will receive A- and so on. The grading is based on the following components:

1. Homeworks (4): 20%
    - Each of the four homeworks is 5%.
    - No grades for late submissions.
    - You are expected to solve the homeworks on your own.
2. Exams (closed book/notes, no make-up exams): 60%
    - Midterm: 25%
    - Comprehensive Final: 35%
3. Projects (2): 18%
    - Project 1: 8% (10% for EDGE students)
    - Project 2: 10%
    - No grades for late submissions.
    - You are expected to complete the projects on your own.
4. Participation: 2% (EDGE students cover it in Project 1).

Homeworks and projects should be submitted using e-Learning before the deadline. Grading will be based on what you explicitly stated in your answers of your homework, exam, or project. Please try to be as clear and precise as possible.

**EDGE** students will be given extra three days compared to on-campus students to finish all the assignments and projects. However, EDGE students will be given only one extra day for both midterm and final compared to the on-campus examination date.

**Grade Requirements for Graduation:** In order to graduate, graduate students must have an overall GPA and an upper-division GPA of 3.0 or better (B or better). Note: a B- average is equivalent to a GPA of 2.67, and therefore, it does not satisfy this graduation requirement. For more information on grades and grading policies, please visit:

https://catalog.ufl.edu/ugrad/current/regulations/info/grades.aspx

**Regrading Policy:** Regrading request should be made within a week from the date the graded item (exam, project, or homework) is available.

**Participation:** I encourage all on-campus students to attend all the lectures and actively participate in class discussions.

**Cell Phones:** Please turn your cell phone off before you come to class.

**Make-up Exam Policy:** No make-up exams except for medical emergencies with supporting documents.

**Honesty Policy:** All students admitted to the University of Florida have signed a statement of academic honesty committing themselves to be honest in all academic work and understanding that failure to comply with this commitment will result in disciplinary action. This statement is a reminder to uphold your obligation as a UF student and to be honest in all work submitted and exams taken in this course and all others.

**Accommodation for Students with Disabilities:** Students Requesting classroom accommodation must first register with the Dean of Students Office. That office will provide the student with documentation that he/she must provide to the course instructor when requesting accommodation.
**UF Counseling Services:** UF Counseling Services. Resources are available on-campus for students having personal problems or lacking clear career and academic goals. The resources include:
UF Counseling & Wellness Center, 3190 Radio Rd, 392-1575, psychological and psychiatric services.
Career Resource Center, Reitz Union, 392-1601, career and job search services.

**Software Use:** All faculty, staff and student of the University are required and expected to obey the laws and legal agreements governing software use. Failure to do so can lead to monetary damages and/or criminal penalties for the individual violator. Because such violations are also against University policies and rules, disciplinary action will be taken as appropriate. We, the members of the University of Florida community, pledge to uphold ourselves and our peers to the highest standards of honesty and integrity.

**Instructor Biography:** Prabhat Mishra is an Associate Professor in the Department of Computer and Information Science and Engineering (CISE) at the University of Florida (UF) where he leads the CISE Embedded Systems Lab. His research interests include design automation of embedded systems, energy-aware computing, hardware/software verification, and design of trustworthy systems. He received his B.E. from Jadavpur University, Kolkata in 1994, M.Tech. from the Indian Institute of Technology, Kharagpur in 1996, and Ph.D. from the University of California, Irvine in 2004 -- all in Computer Science. Prior to joining University of Florida, he spent several years in various semiconductor and design automation companies including Intel, Motorola, Synopsys and Texas Instruments. He has published four books, ten book chapters and more than 100 research articles in premier international journals and conferences. His research has been recognized by several awards including the NSF CAREER Award from the National Science Foundation, two best paper awards (VLSI Design 2011 and CODES+ISSS 2003), five best paper award nominations, and 2004 EDAA Outstanding Dissertation Award from the European Design Automation Association. He has also received the 2007 International Educator of the Year Award from the UF College of Engineering for his significant international research and teaching contributions. Prof. Mishra currently serves as an Associate Editor of ACM Transactions on Design Automation of Electronic Systems (TODAES), IEEE Design & Test of Computers (D&T), IET Computers & Digital Techniques (CDT), and Journal of Electronic Testing (JETTA), Guest Editor of IEEE Transactions on Computers (TC), and as a technical program committee member of several ACM and IEEE conferences including DAC, ICCAD, DATE, ASPDAC, CODES+ISSS, RTAS and VLSI Design. He has also served as General Chair of IEEE High Level Design Validation and Test (HLDVT) 2010, Program Chair of HLDVT 2009, Information Director of ACM TODAES, and Guest Editor of IEEE D&T, Springer JETTA and IJPP. He is a senior member of both ACM and IEEE.